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Design of a 2.4 GHz CMOS LNA for Bluetooth Low Energy Application Using 45 nm Technology

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DESIGN OF A 2.4 GHZ CMOS LNA FOR BLUETOOTH LOW ENERGY APPLICATION USING 45 NM TECHNOLOGY

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ABSTRACT

DESIGN OF A 2.4 GHZ CMOS LNA FOR BLUETOOTH LOW ENERGY APPLICATION USING 45 NM TECHNOLOGY

by Chin-To Hsiao

With the increasing need for the Internet of things (IoT), Bluetooth low energy (BLE) technology has become a popular solution for wireless devices. The purpose of this thesis was to design a complementary metal-oxide-semiconductor (CMOS) low noise amplifier (LNA) for the Bluetooth low energy (BLE) front-end circuit. Forty-five nm CMOS technology was chosen for the design. The schematic was implemented in Cadence Virtuoso Schematic XL using the generic processing design kit (GPDK) 45 nm library and was simulated using Analog Design Environment (ADE). The LNA presented in this thesis achieved the lowest power consumption of 1.01 mW with a supply of 1 V. The LNA provided a reasonable gain which was 14.53 dB. Although the third-order input intercept point (IIP3) was low, which was -10.67 dBm, the noise figure (NF) achieved the lowest value, which was 0.98 dB at the center frequency of 2.44 GHz. This thesis emphasizes that CMOS RF front-end design, amplifier's gain, linearity, and NF play critical roles in defining the circuit's performance.

ACKNOWLEDGEMENTS

First of all, I would like to thank my thesis advisor, Dr. Sotoudeh Hamedi-Hagh, for giving me the opportunity to conduct this research. The door to Prof. Hamedi-Hagh's office was always open whenever I ran into a problem or had a question about my research. His lectures in analog IC design allowed me to have a solid background knowledge in circuit analysis and design.

Secondly, I must thank Dr. Marshall Wang, who is on my thesis committee, for his advising and comments on the paper. His lectures on RFIC design allowed me to have a thorough view of RF circuit design and specification of Bluetooth applications. Moreover, I would like to thank Dr. Lili He, who is also on my thesis committee, for her fantastic lecture in semiconductor devices helped me to establish the cornerstone of my study in analog circuit design.

Above all, I would like to thank my dear grandfather, Tai-Pin Hsiao, who passed away in 2012, for financially supporting me to study in the US. Also, I must express my very profound gratitude to my mother, Hsiu-Chu Lee, for providing me with unfailing support and unceasing encouragement throughout my life. Especial thanks to my beloved girlfriend, Joy Jubane, who had patiently proofread the paper several times without complaint. She was a selfless cheerleader that was always right there when I needed her. Last but not least, my classmate and friend, Uditha Perera, for supporting me through the graduate program as a mentor. This accomplishment would not have been conceivable without them.

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Chapter 1

Introduction

Complementary metal-oxide-semiconductor (CMOS) technology has become popular in wireless applications since the scaling of technology has become smaller, highly integrable, and more affordable. In recent years, wireless technology has been implemented in cosmopolitan applications, not just for consumer electronics, but healthcare sensors such as body temperature and heart rate sensors. Bluetooth low energy (BLE) technology has been implemented in this new trend of instant body information monitoring using portable and wireless devices. The BLE technology that is applied in many electronic devices consumes less power in comparison to classic Bluetooth (BT).

There are ways to improve the energy efficiency of BLE devices. The first step is understanding the physical layer of the design. The next step is to optimize the circuit design such that it gives better performance in terms of power consumption. In BLE's physical layer, the front-end receiver circuit plays a major role in passing the analog signals received through many stages. This thesis concentrates on the initial design stage of the front-end circuit. The purpose was to minimize power consumption and satisfy BLE standards.

The first stage of the BLE front-end receiver circuit is the low noise amplifier (LNA). An LNA design can be divided into five different parts: topologies, input matching network, source degeneration feedback circuit, biasing circuit, and output matching network. Generic processing design kit (GPDK) 45 nm processing technology was used to implement the circuit. Additionally, the key to successfully designing an LNA involves

understanding performance parameters and the resistors, inductors, and capacitors (RLC) circuit theory.

Finally, comparing this thesis to other work is necessary to reevaluate the performance of the LNA circuit. Improvement of the LNA design can be easily seen via power consumption parameters and other key factors such as gain and linearity.

Chapter 2

Bluetooth Technology

2.1 Introduction

With the increasing need for the Internet of things (IoT) in daily lives, BT technology has become a popular solution for portable devices [1]. It is used in mobile phones, medical sensors, and many other consumer electronics. The main reason that BT was the best candidate for IoT compared to other wireless devices was the introduction of the energy saving feature, BLE.

2.2 Key Factors of BLE

The key elements that allow BLE to have the lowest cost possible are the industrial, science, and medical (ISM) band, IP license, and low power [2]. One major advantage of using the ISM band is that a permit or fee is not required, although it must follow a specific power requirement for data transmission. The maximum power fed into the antenna must be lower than 30 dBm (equivalent to 1W) [2]. The BT special interest group (SIG) provides a reasonable price for an IP license, which is relatively lower than other competitors [2]. The cost of the license can be reduced, because an increasing number of customers and users are supporting BLE devices.

Low power is necessary for mobile devices because consumers are expected to use the devices for extended periods without charging or changing the power source. Making a sustainable device requires more energy storage, low power consumption, or both. However, the energy storage in the device demands additional space. The large device size also meant that manufacturing costs were higher, so increasing the energy storage

was an inefficient solution for long-period usage. Therefore, lowering the power of the device not only reduces manufacturing cost but also improves battery usage. Since more power is needed for the device, more space is preserved for the power source or battery.

Even though low power is suitable for the device, sometimes the device needs to operate at high speeds for some specific applications. Therefore, BT version 4.0 was introduced to combine the needs of different usage modes, which led to a solution that allowed for BT to have three operation modes.

2.3 Operation Modes

After BT had evolved to version 4.0, it had three different modes, which are classic BT, BLE, and dual-mode [3]. The Bluetooth Smart Ready mark represents the dual-mode, the Bluetooth mark represents the classic BT mode, and the Bluetooth Smart mark represents BLE mode [4].

Classic BT was initially designed to connect two devices at a short distance for transferring data, such as linking mobile phones to computers. Furthermore, the application was improved to not only transfer data but also to stream audio and video. This improvement provided a robust wireless connection between devices ranging from smartphone and car audio devices to industrial controllers and medical sensors. However, BLE became a more power efficient and cost effective solution for many of these applications.

When comparing BLE to classic BT, the main difference is power dissipation. The BLE devices manage to operate for extended periods of time. This advantage is beneficial in machine to machine (M2M) communication because it can last for years without

changing the power source once the BLE device is placed in the machine. However, to achieve this goal, the data transmission rate must be sacrificed in exchange for low power dissipation [5].

BLE devices slow down the data transfer rate, though it effectively decreases the power consumption. Unlike classic BT devices, BLE devices do not need to be at the highest speed possible. For example, while one uses the smartphone to switch on the air conditioner and adjust the room temperature, these applications do not have significant data to transfer. It simply needs to send the package containing "power on" and "increase/decrease temperature" from the transmitter to the receiver. On the other hand, while one uses a smartphone to stream television through a BT connection, it is not a simple package containing a single command; instead, it can be a high definition (HD) video or high quality (HQ) music file that must be smoothly played on television. Otherwise, the user will never replace the wired connection with wireless.

2.4 Summary

Chapter 2 discussed the specifications of BT and BLE. The structure of BLE is slightly different from the structure of BT because of the low energy requirements. The ISM band, IP license, and low power are key elements that allow BLE to have the lowest cost possible. The design of BLE was introduced to have an overview of the technology that is utilized in this paper.

Chapter 3

RF Circuit Theory

3.1 Introduction

An RF circuit's characteristics are significantly affected by passive components such as resistors, inductors, and capacitors (RLC). Within the RF circuit, the RLC plays an important role in matching networks. Matching networks consist of passive components which are necessary to eliminate the unwanted effects of RLC. Additionally, maximum power transfer can be achieved using different matching networks.

3.2 RLC Network

Different from other digital circuits, the value of RLC in RF circuits must be extremely precise due to the sensitivity of the frequency response. A slight change of the RLC circuit within the RF circuit can cause a considerable effect that ruins the expected performance. Therefore, the following section comprises a review of the RLC network, which is necessary to design an LNA's matching circuit.

3.2.1 Parallel RLC

The RLC parallel circuit, shown in Figure 3-1, illustrates that the total impedance (Zin) can be expressed as Equation 3.1 [6].

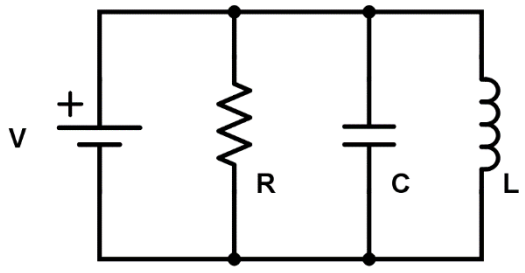


Figure 3-1 RLC parallel circuit with voltage source V. Adapted from [6]

$$Z_{in} = \frac{1}{R} + j\omega C + \frac{1}{j\omega L} = G + j(\omega C - \frac{1}{\omega L}) \tag{3.1}$$

According to Equation 3.1, the circuit is applied to the DC source, which means that the frequency is zero. Ideally, the impedance for capacitor (C) will become infinitely large, as an open circuit, and the impedance of inductor (L) is zero, as a short circuit. When the circuit is applied to the AC source with an extremely high frequency, then the dominant impedance will be L, as an infinite value, and C, as a value close to zero. The objective of distinguishing high and low frequencies is to determine when the C and L impedances cancel out one another. The point at which the C and L values cancel each other out is also called resonant frequency, which can be calculated by Equations 3.2 and 3.3 [6].

$$\left(\omega_0 C - \frac{1}{\omega_0 L}\right) = 0 \tag{3.2}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.3}$$

where ω_0 is resonant frequency.

Impedance will be equal to G in Equation 3.1 at the resonant frequency; however, the current flow through either capacitor or inductor can be relatively large. This outcome is the sign of downward impedance transformation [6]. To further discuss this phenomenon, the quality factor (Q) must be introduced to elaborate on this effect.

3.2.2 Quality Factor (Q)

Instead of resonant frequency, Q is the parameter used to discover the characteristics and performance of the circuit. The most basic definition is embodied in Equation 3.4 [6].

$$Q = \omega \times \frac{Energy\ Stored}{Average\ Power\ Dissipated} \tag{3.4}$$

where ω is angular frequency.

Quality factor (Q) is dimensionless and is proportional to the ratio of energy stored in power dissipation. It is convenient for circuit analysis that one does not need to calculate a specific component's energy, since finding the stored energy of a specific capacitor or inductor can be a difficult task. Therefore, Q is a handy parameter for resonant and non-resonant systems.

At resonant frequency, the total voltage supply V in Figure 3-1 can be expressed as $I_{in}R$. The total energy of the circuit can be calculated by Equation 3.5 [6].

$$E_T = \frac{1}{2}C(I_pR)^2 \tag{3.5}$$

where I_p is the peak current value.

The average power (P_{av}) is relatively straightforward to find since the effect of the capacitor and inductor cancel out each other, as shown in Equation 3.6.

$$P_{av} = \frac{1}{2}{I_p}^2R \tag{3.6}$$

As a result, factor Q can be presented as Equation 3.7 at the resonant frequency.

$$Q = \omega_0\frac{E_T}{P_{av}} = \frac{1}{\sqrt{LC}}\frac{\frac{1}{2}C(I_pR)^2}{\frac{1}{2}{I_p}^2R} = \frac{R}{\sqrt{L/C}} \tag{3.7}$$

Additionally, the impedances of capacitor (X_C) and inductor (X_L) are identical as shown in Equation 3.8.

$$|X_c| = |X_L| = \omega_0 L = \frac{L}{\sqrt{LC}} = \sqrt{\frac{L}{C}} \tag{3.8}$$

Since the $\sqrt{\frac{L}{C}}$ is known as the impedance of the capacitor and the inductor, Equation 3.7 can be rewritten as Equation 3.9.

$$Q = \frac{R}{|Z_{L,C}|} = \omega_0 RC = \frac{R}{\omega_0 L} \tag{3.9}$$

3.2.3 Series RLC

The RLC series circuit, as shown in Figure 3-2, illustrates that the total impedance (Zin) can be expressed as Equation 3.10 [7].

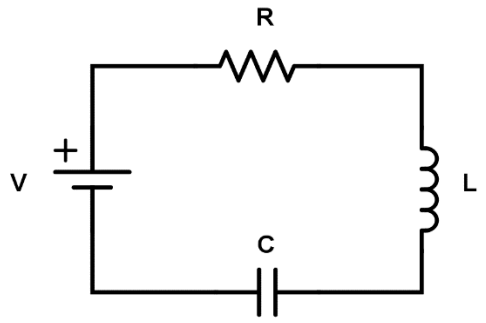


Figure 3-2 RLC series circuit with voltage source V. Adapted from [6]

$$Z_{in} = R + j\omega L + \frac{1}{j\omega C} = R + j(\omega L - \frac{1}{\omega C}) \tag{3.10}$$

When the circuit operates at a resonant frequency, the Zin is the smallest value, which is R. The Q in the RLC series circuit can also be calculated by Equations 3.11 and 3.12, which are the reciprocal forms of Equations 3.7 and 3.9, respectively.

$$Q = \frac{\sqrt{L/C}}{R} \tag{3.11}$$

$$Q = \frac{\omega_0 L}{R} = \frac{1}{RC\omega_0} \tag{3.12}$$

3.2.4 Power Transfer

Power gain operates sufficiently at a low frequency. However, the power gain is usually deficient because of the power loss that occurs when transferring from one stage to the other. Therefore, RF circuit design should focus on impedance transforming. Assuming that the RF circuit is a simple voltage source with a source impedance and a load impedance, as shown in Figure 3-3.

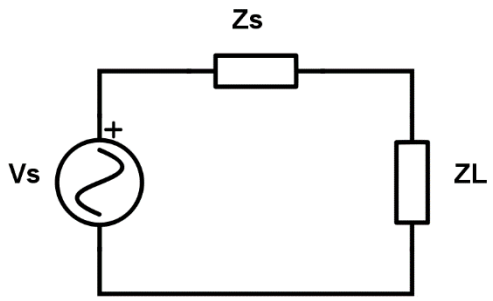


Figure 3-3 Simplified RF circuit as an RLC series circuit. Adapted from [6]

The source impedance (Z_s) can be written as resistor (R_s) in series with an impedance (X_s) while the load impedance can be presented as R_L and X_L. In order to have the maximum power transfer, load power can be presented as Equation 3.13 [6].

$$P_L = \frac{V_L^2}{R_L} = \frac{R_L V_s^2}{(R_L + R_s)^2 + (X_L + X_s)^2} \tag{3.13}$$

In this content, the maximum power transfer will happen when X_s and X_L cancel each other out. Furthermore, R_s must be equal to R_L to minimize the power loss. In order to do so, the following sections, from 3.2.5 to 3.2.7, are three universal ways to match the impedance and optimize the power transmission.

3.2.5 *L*-match Circuit

Before considering the L-match circuit, one must be equipped with the concept of parallel and series impedance circuit transformation, as shown in Figure 3-4. The transformation of impedance Z_{AB} can be derived by Equations 3.14 and 3.15 [8].

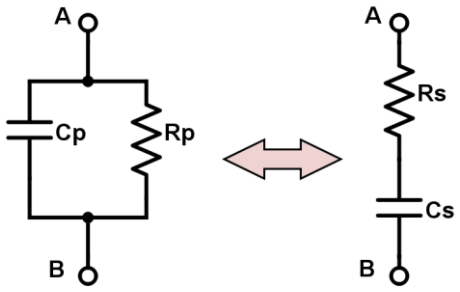


Figure 3-4 Parallel to series circuit transformation. Adapted from [8]

$$R_P = R_s(Q^2 + 1) \tag{3.14}$$

$$X_P = X_s\left(\frac{Q^2 + 1}{Q^2}\right) \tag{3.15}$$

Where $X_P = \frac{1}{\omega C_P}$ and $X_S = \frac{1}{\omega C_S}$, these two transform equations will provide the critical concept to understand the L-match circuit. In the L-match circuit, the load impedance can

be presented as upward or downward, as shown in Figure 3-5. Both R_S and R_P can be transformed into each other using Equation 3.16 [6].

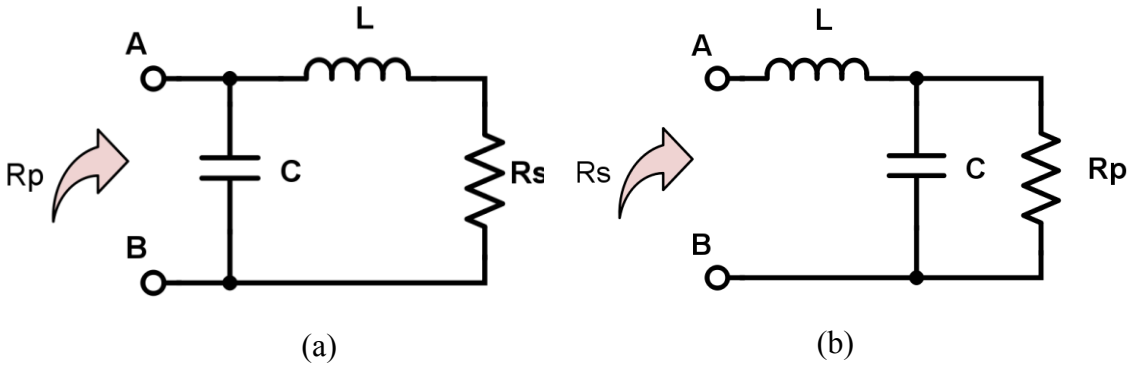


Figure 3-5 L-match circuit (a) upward (b) downward. Adapted from [6]

$$R_P = R_s(Q^2 + 1) \tag{3.16}$$

Since R_s is in parallel with C, the $Q = (\frac{1}{\omega_0 R_s C})$. Also, assume the Q^2 is greater than 1 to simplify the equation. The approximate value of R_P can be rewritten as Equation 3.17.

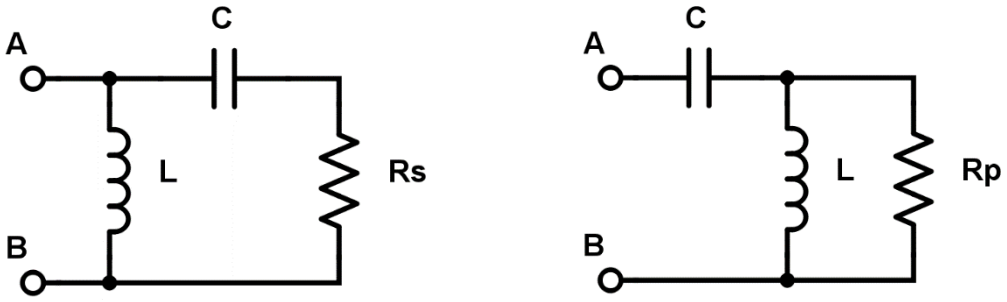
$$R_P \cong \frac{1}{R_s}\frac{L}{C} \tag{3.17}$$

From Equation 3.16, Q can also be rewritten in terms of the ratios of R_s and R_P as Equation 3.18. The $\frac{R_P}{R_s}$ is also known as transformation ratios [6].

$$Q \cong \sqrt{\frac{R_P}{R_s}} \tag{3.18}$$

Finally, because the impedance conjugate matches, two reactances do not vary much during the transformation. Thus, changing the position of the inductor and capacitor will not affect the circuit significantly. This conclusion is helpful when facing the impedance matching problems; the designers can manipulate the position of impedances to

implement the high-pass or low-pass circuit. When the circuit operates at high frequency, Figure 3-5 reacts as an open circuit. Therefore, these two circuits are used as the low-pass circuit. For high-pass circuit application, all that should occur is switching the positions of capacitor and inductor, as shown in Figure 3-*6*.



(a) (b)

Figure 3-6 High-pass L-match circuit (a) upward (b) downward. Adapted from [6]

3.2.6 *π*-match Circuit

The π-match circuit is introduced to improve the limitation of L-match circuit. The limitations can be specified into three parts which are center frequency, impedance transformation ratio, and Q [6]. L-match circuit has only two components to manipulate these three limitations. However, π-match circuit adds one more component to give the designers more freedom to optimize the circuit, as shown in Figure 3-7.

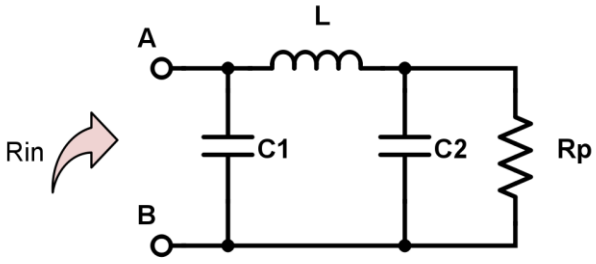


Figure 3-7 π-match circuit with one inductor, one resistor, and two capacitors. Adapted from [6]

As the previous section showed the characteristics of L-match circuit, Figure 3-7 can be separated into two parts which are upward L-match and downward L-match circuit, as shown in Figure 3-8.

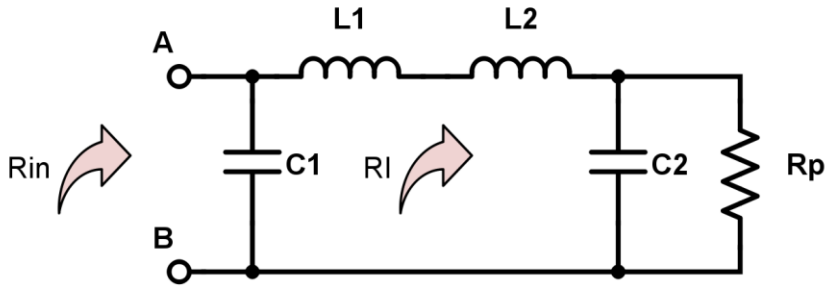


Figure 3-8 π-match circuit using two back to back L-match circuits. Adapted from [6]

The parallel resistor R_P is not in the same path as inductor L_2 which consequently makes it difficult to observe the resonant effect. The parallel and series impedance circuit transformation technique is used to transform the R_P and C_2 to R_I and C_{2S}, as shown in Figure 3-9.

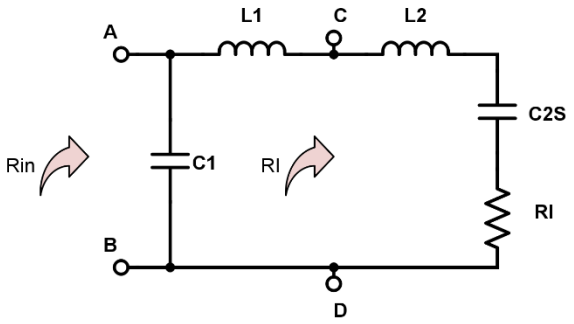


Figure 3-9 Transformation from R_P and C_2 to R_I and C_{2S}

The L_2 and C_{2S} cancel each other out due to the resonant effect, so the resistance observed from node CD is R_I. Based on Equation 3-13, the simple RLC series circuit is seen from node CD. The Q_{CD} can be presented in terms R_I and R_P as shown in Equation 3.19.

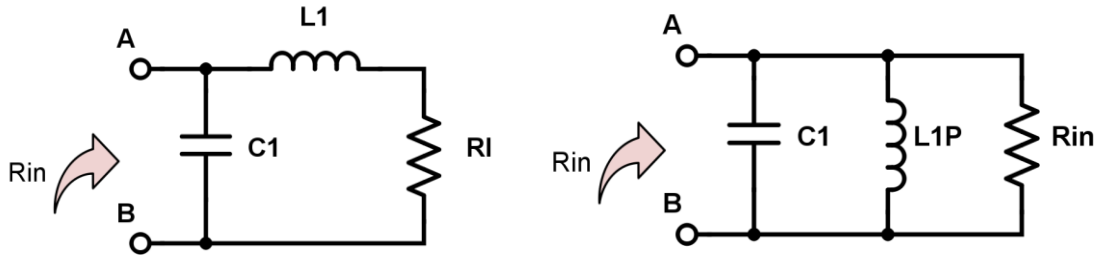
$$Q_{CD} = \frac{\omega_0 L_2}{R_I} = \sqrt{\frac{R_P}{R_I} - 1} \tag{3.19}$$

where the $\frac{R_P}{R_I}$ is the transformation ratio.

When considering the circuit from node AB, the circuit can be further simplified as shown in Figure 3-10. Similar to the previous section, all the components must be on the same path, which is either series or parallel. Therefore, the circuit shown in Figure 3-10 (a) can be transformed to Figure 3-10 (b) to find the final equation for the π-match circuit. The R_{in} can be written in terms of R_I, as shown in Equation 3.20, and the L_{1P} can expressed in terms of L_1, as shown in Equation 3.21 [6].

$$R_{in} = R_I(Q_{AB}^2 + 1) \tag{3.20}$$

$$L_{1P} = L_1 \frac{(Q_{AB}^2 + 1)}{Q_{AB}^2} \tag{3.21}$$



(a) (b)

Figure 3-10 Transformation from (a) RL series circuit to (b) RL parallel circuit. Adapted from [6]

The Q_{AB} can be derived from Equations 3.20 and 3.21 as shown in Equation 3.22.

$$Q_{AB} = \frac{\omega_0 L_1}{R_I} = \sqrt{\frac{R_{in}}{R_I} - 1} \tag{3.22}$$

The overall network Q_{ov} is a summary of Q_{AB} and Q_{CD} as shown in Equation 3.23.

$$Q_{ov} = Q_{AB} + Q_{CD} = \frac{\omega_0 (L_1 + L_2)}{R_I} = \sqrt{\frac{R_{in}}{R_I} - 1} + \sqrt{\frac{R_P}{R_I} - 1} \tag{3.23}$$

Additionally, the inductor $L_1 + L_2$ and capacitors C_1 and C_2 can be found by Equations 3.24, 3.25, and 3.26.

$$L_1 + L_2 = \frac{Q_{ov}}{\omega_0 R_I} \tag{3.24}$$

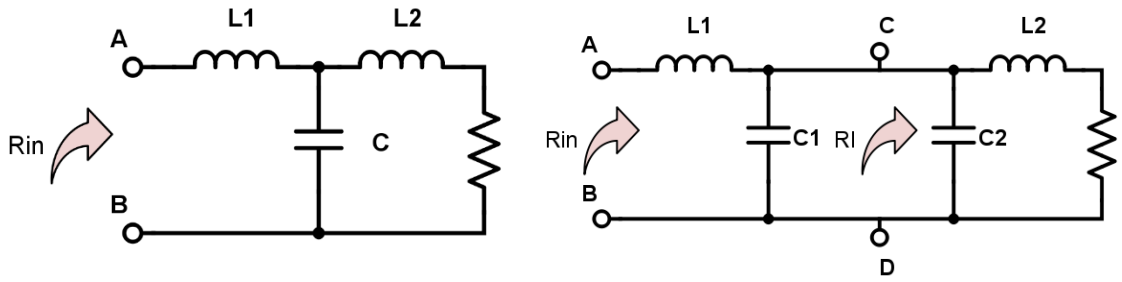
$$C_1 = \frac{Q_{AB}}{\omega_0 R_I} \tag{3.25}$$

$$C_2 = \frac{Q_{CD}}{\omega_0 R_P} \tag{3.26}$$

Lastly, the most common reason for using a π-match circuit is to improve the effect of parasitic capacitors [6]. To estimate the bandwidth and operating frequency, designers must know the impedance of the network. However, the parasitic capacitors are the invisible and inevitable factor that keeps affecting the circuit. The π-match circuit can absorb most of the parasitic capacitors into the network. Therefore, with the purpose to ensure the bandwidth and operating frequency remain robust, the π-match circuit is conveniently applied to the circuit.

3.2.7 *T*-match Circuit

Another method to match the impedance is T-match circuit, as shown in Figure 3-11 (a). It shares the same concept of connecting two L-match circuits back to back. The capacitor C can be viewed as two parallel capacitors, C_1 and C_2, as shown in Figure 3-11 (b). The fundamental formula of Q, C, and L for T-match circuit can be derived from the π-match circuit, as shown in Equations 3.27, 3.28, 3.29, and 3.30 [6].



(a) (b)

Figure 3-11 Transformation from (a) T-match circuit to (b) two back to back L-match circuits. Adapted from [6]

$$Q_{ov} = Q_{AB} + Q_{CD} = \omega_0 R_I (C_1 + C_2) = \sqrt{\frac{R_I}{R_{in}} - 1} + \sqrt{\frac{R_I}{R_S} - 1} \tag{3.27}$$

$$C_1 + C_2 = \frac{Q_{ov}}{\omega_0 R_I} \tag{3.28}$$

$$L_1 = \frac{Q_{AB} R_{in}}{\omega_0} \tag{3.29}$$

$$L_2 = \frac{Q_{CD} R_S}{\omega_0} \tag{3.30}$$

T-match circuits are used mainly when the voltage source and the load are inductive. The matching circuit can absorb the parasitic inductors to the matching network.

3.3 Summary

Understanding the characteristics of RLC circuits is vital to calculating the input and output impedance of the network. In LNA design, input and output matching networks are essential for transferring data. In order to obtain the maximum power transfer, constructing a matching network is neccesary, since it leads to minimum loss allowing for more efficiency.

Chapter 4

2-Port Network, Bandwidth, and Noise

4.1 Introduction

In Chapter 4, the 2-port network, bandwidth, and noise are introduced. S-parameter provides the standards that define the performance of the network, such as gain and reflection rate. S-parameter can be derived from a 2-port network using simple current, voltage, and impedance relationship. The bandwidth estimation technique's purpose is to ensure that the RF circuit performs at the desired operation frequency. Also, the different types of undesired signal, noise, will be introduced.

4.2 2-port Network

The 2-port network is a universal way to analyze an RF circuit [9]. A "black box" is used to represent a 2-port network, as shown in Figure 4-1. This network does not discuss the details inside the box, but the applied voltage and current flow to port 1 and port 2, as shown in Equations 4.1 and 4.2. In this case, based on the values observed from the network, the characteristics of the circuit can be found without analyzing the whole circuit.

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \tag{4.1}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{4.2}$$

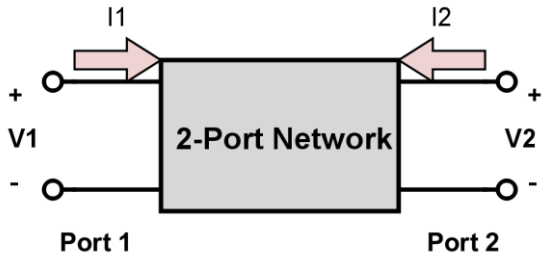


Figure 4-1 2-port network with voltage source V1 and V2

4.2.1 Y-parameters

Y-parameters are called short-circuit admittance parameters [9]. In Figure 4-1, V_1 and V_2 are selected as independent variables and I_1 and I_2 are dependent variables. Some analysis was needed to define the four parameters: Y_{11}, Y_{22}, Y_{12}, and Y_{21}. Each individual analysis was made with respect to one port of the network triggered by a voltage source. Simultaneously, the other port is short circuited, as shown in Equations 4.3, 4.4, 4.5, and 4.6 [9]. Y-parameters express the port currents in terms of port voltages.

$$Y_{11} = \frac{I_1}{V_1}\Big|_{V_2=0(\text{Input admittance with port 2 shorted})} \tag{4.3}$$

$$Y_{22} = \frac{I_2}{V_2}\Big|_{V_1=0(\text{Output admittance with port 1 shorted})} \tag{4.4}$$

$$Y_{12} = \frac{I_1}{V_2}\Big|_{V_1=0(\text{Reverse transfer admittance with port 1 shorted})} \tag{4.5}$$

$$Y_{21} = \frac{I_2}{V_1}\Big|_{V_2=0(\text{Forward transfer admittance with port 2 shorted})} \tag{4.6}$$

If I_1 and I_2 are selected as independent variables and V_1 and V_2 are taken as dependent variables, the network can be distinguished using two linear equations as shown in

Equations 4.7 and 4.8. However, Z-parameter sets provide the same information about a network.

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \tag{4.7}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \tag{4.8}$$

4.2.2 S-parameters

Scattering parameters, which are also known as S-parameters, are a parameter set that relays information on traveling waves. These waves are scattered or reflected when an n-port network is introduced to a transmission line [10]. S-parameter is widely used to analyze transistor circuits, amplifiers, and other active devices. For example, they are usually measured with RF circuits and the instrument is embedded between a 50 Ω load and source [11].

S-parameters are a common way to describe a network. Unlike terminal voltages and currents, the traveling waves do not change in comparison to the magnitude at terminals along a transmission line [10]. S-parameters can then be measured on a wireless device located at a certain distance. The distance from the measurement transducers provide the measuring device for transmission lines.

The 2-port network is used to define S-parameters as shown in Figure 4-2. The variables a_1 and a_2 are normalized incident voltages, as shown in Equations 4.9 and 4.10 [10].

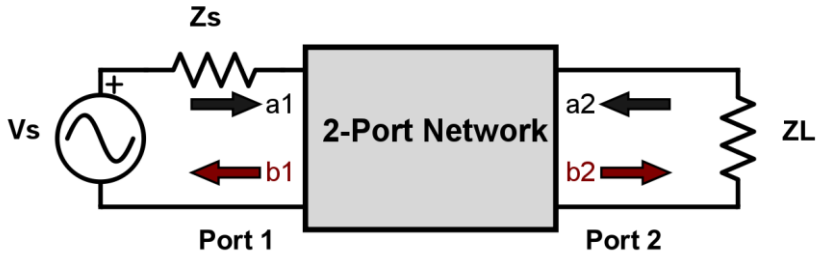


Figure 4-2 2-port network with incident waves (a1, a2) and reflected waves (b1, b2) used in s-parameter definitions. Adapted from [10]

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave incident on port 1}}{\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}} \tag{4.9}$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave incident on port 2}}{\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}} \tag{4.10}$$

where Z_0 refers to a single positive real impedance.

While the dependent variables b_1 and b_2 are normalized reflected voltages, as shown in Equations 4.11 and 4.12.

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave reflected on port 1}}{\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}} \tag{4.11}$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave reflected on port 2}}{\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}} \tag{4.12}$$

The equations that represent the 2-port network are Equations 4.13 and 4.14.

$$b_1 = S_{11} a_1 + S_{12} a_2 \tag{4.13}$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \tag{4.14}$$

Finally, the S-parameters are defined by Equations 4.15, 4.16, 4.17, and 4.18.

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0(\text{Port 1 reflection with port 2 terminated by a match load } Z_L=Z_0)} \tag{4.15}$$

$$S_{22} = \frac{b_2}{a_2}|_{a_1=0(\text{Port 2 relection rate with port 1 terminated by a matched load})} \tag{4.16}$$

$$S_{12} = \frac{b_1}{a_2}|_{a_1=0(\text{Reverse transmission gain with port 1 terminated in a matched load})} \tag{4.17}$$

$$S_{21} = \frac{b_2}{a_1}|_{a_2=0(\text{Forward transmission gain with port 2 terminated in a matched load})} \tag{4.18}$$

S-parameters S_{11} and S_{22} are identical to optical reflection coefficients; S_{12} and S_{21} are identical to optical transmission coefficients. Overall, S-parameters help designers to predict circuit behavior in terms of the desired performance.

The above-mentioned relationship which was between reflection coefficient and impedance is the primary deciding factor of the Smith chart transmission line calculator. Subsequently, the reflection coefficients S_{11} and S_{22} can be plotted on Smith charts. These parameters can then be converted directly to impedance and easily manipulated to determine matching networks for optimizing circuit design.

4.2.3 Smith Chart

The Smith chart is a common way to apply impedance matching on a transmission line, it also shows the reflectances on the chart. The reflection coefficients can be presented regarding impedance as shown in Equation 4.19 [6][12]. The equation can be rewritten regarding normalized load impedance Z_{nL}.

$$\Gamma = \frac{\frac{Z_L}{Z_0} - 1}{\frac{Z_L}{Z_0} + 1} = \frac{Z_{nL} - 1}{Z_{nL} + 1} \tag{4.19}$$

In Equation 4.19, the relationship between impedance and Γ are a map of one complex number to another. It is also called bilinear transformation since the ratio of the two functions are linear. An essential concept of bilinear transformation is that a line on the

map can be considered as a circle with infinite radius [6][12]. As shown in Figure 4-3, the unit circle in the Γ-plane maps into lines representing an imaginary axis in the Z-plane.

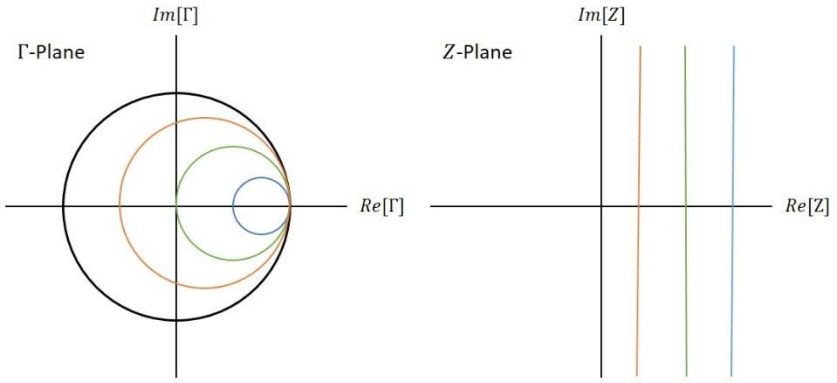


Figure 4-3 Mapping of circles in Γ-plane to constant-resistance lines in Z-plane. Adapted from [6]

Lines of constant reactance are orthogonal to lines of constant resistance in the Z-plane, and this orthogonality is preserved in the mapping. We can expect constant-reactance lines to transform into circular arcs, as shown in Figure 4-4. The Smith chart is the plotting of both constant-resistance and constant-reactance contours in the Γ-plane without the explicit presence of the Γ-plane axis.

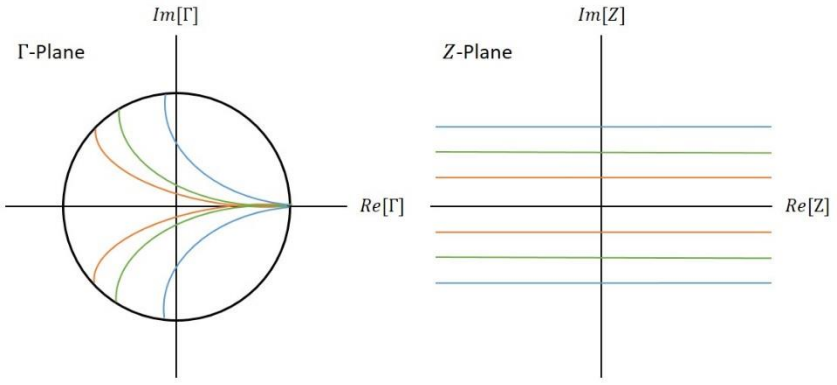


Figure 4-4 Mapping of contours in Γ-plane to constant-reactance lines in Z-plane. Adapted from [6]

The Smith chart can be found on computer aided design (CAD) tools to help designers see the matching problem clearly and easily.

4.3 Bandwidth

Bandwidth is another critical factor in circuit design, especially for RF circuits. Different wireless products must work at various frequencies. For example, the frequency band for Bluetooth technology is from 2.4000 GHz to 2.4835 GHz [3]. Using hand calculations to estimate the bandwidth of an RF circuit is a difficult job that requires one to find not only the peak frequency (f_{peak}), but also the -3dB point of the circuit, as shown in Figure 4-5. In order to find these values, the total impedance of the circuit must be established first. The total impedance takes into consideration the input, output, and any other voltage sources in the circuit. It is more difficult to find the impedance at each node in the circuit because there are many parasitic capacitors and on/off chip inductors. However, the conventional way to find the impedance is called open-circuit time constant (OTC), also known as zero value time constant [6].

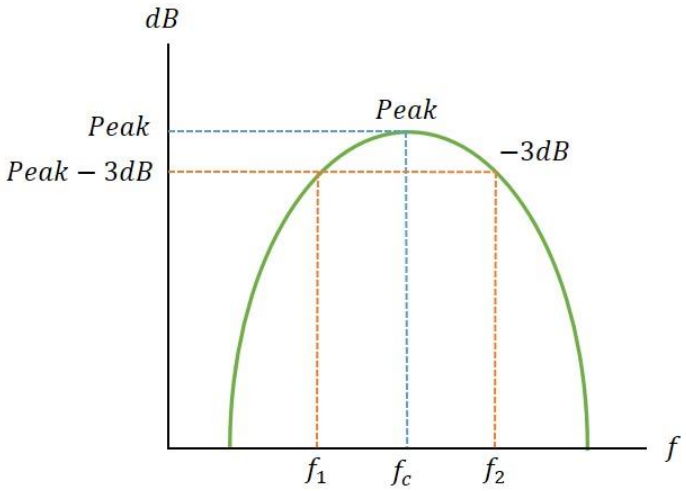


Figure 4-5 Bandwidth diagram example with $-3dB$ points and peak frequency f_{peak}

OCT allows designers to estimate the bandwidth of a system by inspection from nodes; however, this method is an ineffective way of precision estimation and depends heavily on processing technology. The processing technology is used with regards to manufacturing quality and precision. One major advantage of OCT is to indicate the elements that are responsible for bandwidth limitations [6].

All-pole transfer functions are needed to discuss the OCT, assuming that a system function can be written as Equation 4.20 [6].

$$\frac{\mathrm{V}_o(s)}{V_i(s)} = \frac{a_0}{(\tau_1 s + 1)(\tau_2 s + 1) \ldots (\tau_n s + 1)} \tag{4.20}$$

The multiplying terms of time constants $(\tau_1 s + 1)(\tau_2 s + 1) \ldots (\tau_n s + 1)$ can be expressed as $b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + 1$, where b_n represents the products of time constants.

While it is at the -3dB point, the first-order term b_1 dominates the other terms. Therefore, the Equation 4.20 can be approximately simplified as Equation 4.21 [6].

$$\frac{\mathrm{V}_o(s)}{V_i(s)} \approx \frac{a_0}{b_1 s + 1} = \frac{a_0}{(\sum_{i=1}^{n} \tau_i) s + 1} \tag{4.21}$$

The radian frequency of this system can be found easily as a reciprocal of the approximate time constant b_1, as shown in Equation 4.22.

$$\omega_h \approx \frac{1}{b_1} = \frac{1}{\sum_{i=1}^{n} \tau_i} \tag{4.22}$$

Four steps can be applied to find the pole (ω_h) of the circuit:

1. Keep one of the capacitors in the circuit (C_j)

2. Open all other capacitors
3. Find resistance (R_j) across the (C_j)
4. Repeat above steps for another capacitor in the circuit

Finally, the sum of OTC is formed in step 4, as shown in Equation 4.23.

$$\omega_h \approx \frac{1}{\sum_{j=1}^{m} R_{j0} C_j} \tag{4.23}$$

4.4 Noise

Noise is an undesired and unavoidable signal that occurs in electronic and RF circuits. Noise can come in many forms, such as thermal noise, shot noise, and flicker noise [6]. Therefore, it is necessary to differentiate and define how noise is generated so that the unwanted effects of noise can be minimized to an acceptable degree. Unfortunately, it is impossible to eliminate noise. Although there are several types of noise, this section focuses on three major types.

4.4.1 Thermal noise

Thermal noise is random in nature, with no form of prediction [6][13]. This noise is generated because of the agitation of the charge carriers, which are electrons within an electrical conductor. The applied voltage does not affect the level of thermal noise because the charge carriers will only vibrate due to temperature variation. Which means that the higher the temperature, the higher the agitation, and results in higher thermal noise level.

Thermal noise is categorized as a white noise that extends over a broad spectrum. The noise power is proportional to the bandwidth. Therefore, a generalized equation of the noise voltage within a given bandwidth can be defined as shown in Equation 4.24.

$$V_n^2 = 4KT \int_{f1}^{f2} R \, df \tag{4.24}$$

where:

V_n is noise voltage integrated RMS voltage between frequencies f_1 and f_2

R is resistive component of the impedance (or resistance) Ω

T is temperature in degrees Kelvin

f_1, f_2 are lower and upper limits of required bandwidth

For most cases, the resistive component of the impedance will remain constant over the required bandwidth. Therefore, Equation 4.24 can be simplified into Equation 4.25 [6].

$$V_n = \sqrt{4KT\Delta fR} \tag{4.25}$$

where Δf is bandwidth in Hz.

4.4.2 Shot Noise

Shot noise explains the phenomena of discrete movement regarding light and electric currents. To further understand the concept of shot noise, imagine that a laser pointer emits light with a stream of discrete photons to create a visible spot on the wall. Billions of photons are required to have enough brightness to create a spot. However, theses photons are emitted from the laser at random times causing minute variations through time. The minute changes may affect the outcome in which the brightness of the laser is reduced until only a few photons are hitting the wall. This fluctuation in some photons can be called shot noise [6].

The same concept is applied to electric currents. The charge carried by electrons in a circuit also contributes a slight amount of noise. The charges come in discrete bundles that are discontinuous pulses of current; this phenomenon occurs when an electron hops an energy barrier. Therefore, shot noise can be observed because of the difference of the arrival times. Equation 4.26 provides a universal way to explain shot noise [6].

$$I_n^2 = 2qI_{DC}\Delta f \tag{4.26}$$

where:

I_n is RMS noise current in bandwidth

q is electronic charge

I_{DC} is DC current through an energy barrier

Δf is bandwidth in Hz

4.4.3 Flicker noise

Flicker noise is widely known as pink noise and is a form of noise that exhibits an inverse frequency power density curve with a characteristic of $1/f$. However, there is no universal mechanism to explain flicker noise. In an electric network, the flicker noise occurs when there is a variation in the voltage or current, causing the variation of resistors [6][13].

For an electronic device flicker noise mainly happens at low frequencies and white noise contributes at high frequencies. The boundary can be set by the corner frequency f_c, as shown in Figure 4-6.

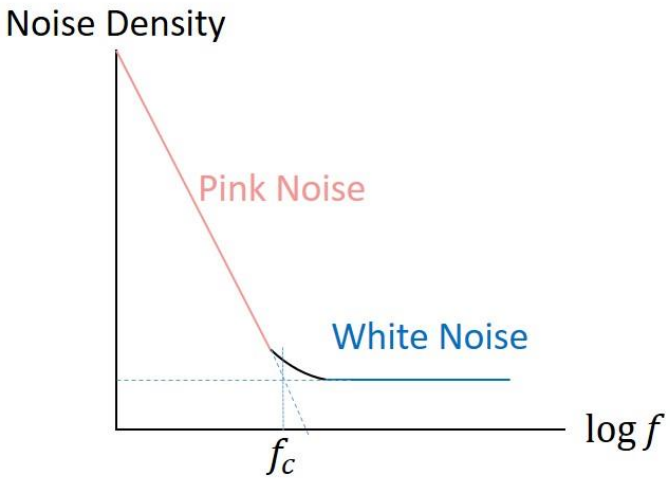


Figure 4-6 The relationship of white noise, pink noise, and corner frequency f_c. Adapted from [6]

In many electronic applications such as RF oscillators, flicker noise dominates the low-frequency region and the white noise from sources such as shot noise and thermal noise dominate the high-frequency region. As flicker noise is proportional to the inverse frequency, the noise equation can be expressed as Equation 4.27 [6].

$$N^2 = \frac{K}{f^n}\Delta f \tag{4.27}$$

where:

N is RMS noise signal that can be either voltage or current

K is empirical parameter that is device specific

n is exponent that is close to unity

Δf is bandwidth in Hz

4.5 Summary

S-parameter is used to determine a circuit's performance which can be easily seen. With the bandwidth estimation technique, the circuit designers can make the circuit more efficient at the operation frequency. However, the noise is an inevitable interference that must be considered in circuit design.

Chapter 5

LNA Design Parameters

5.1 Introduction

Based on the RF circuit design theory introduced in Chapter 3 and 4, LNA design factors will be discussed in this chapter. LNA is the first stage of the front-end receiver after the antenna; the front-end receiver structure is shown in Figure 5-1[14]. The key factors of LNA, such as noise figure, gain, and linearity are introduced to understand what compromises are needed to achieve the goal. It is essential for the BLE front-end circuit to be equipped with high noise immunity, low-power consumption, and reasonable gain. The details of the LNA design factors will be elaborated in the following sections.

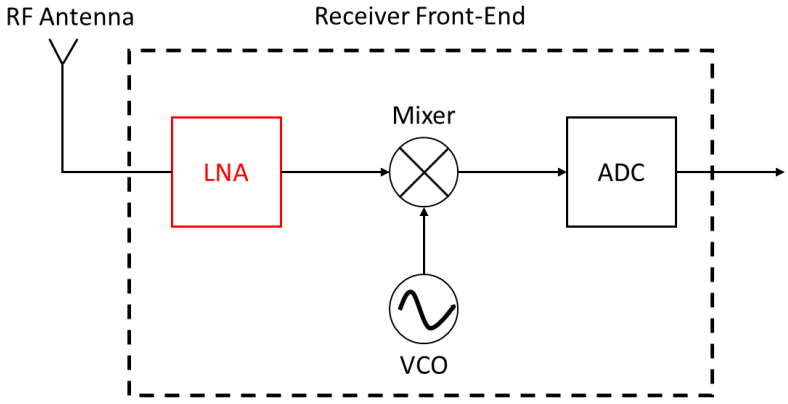


Figure 5-1 Simplified structure of the front-end receiver network.

5.2 Noise Properties

Measuring noise properties in a network or system is necessary to minimize the noise issues that are generated from the receiver. One simple solution for this is to ensure that the receiving signal is strong enough to surpass the noise. Another approach is to minimize the noise produced by the receiver components. However, a reliable noise

measuring method must be established first to address the noise problem. This method must be accurate and straightforward. Therefore, the noise figure (NF), developed by Harold Friis in the 1940s [15], was created to determine the noise immunity of a system in the certain frequency band.

5.2.1 Noise Figure (NF)

There is a myriad of noise types that exist in nature as mentioned in section 4.4; it is tedious and almost impossible to interpret each noise type in an RF circuit. Therefore, in a communication system, NF is straightforward and measurable for designers to see the effect of the noise in a system.

The definition of NF can be shown as Equation 5.1 [15].

$$NF = 10 \log F \tag{5.1}$$

where F is the noise factor.

F can be simply defined by Equation 5.2 [15].

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_i/N_i}{S_o/N_o} \tag{5.2}$$

where:

SNR is signal-to-noise ratio

S_i, S_o are signal level available at input and output

N_i, N_o are noise level available at input and output

Based on Equation 5.2, Equation 5.1 can be rewritten as Equation 5.3. Simply, NF is the difference in decibels (dB) between the SNR_{in} and SNR_{out}.

$$NF = 10\log(\frac{SNR_{in}}{SNR_{out}}) = SNR_{in,dB} - SNR_{out,dB} \quad (5.3)$$

Ideally, as the received signals go through the network, the SNR_{in} and SNR_{out} should be identical. This is because the noise and the desired signal from input are amplified by the same gain. SNR_{in} and SNR_{out} will have the same value. Realistically, the receiving network may generate noise itself by its components and degrade the SNR, as shown in Equation 5.4 [15]. An additional noise signal (N_a) and the network gain (G) are added to rewrite Equation 5.2.

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{GS_i/(N_a + GN_i)} = \frac{N_a + GN_i}{GN_i} \quad (5.4)$$

Equation 5.4 represents the F in terms of input noise (N_i), network gain (G), and additional noise (N_a). Consider that N_i is dominated by thermal noise. In this case, Equation 5.4 can be rewritten as Equation 5.5 [15].

$$F = \frac{N_a + KT_0BG}{KT_0BG} \quad (5.5)$$

where:

K is $1.38\times10^{-23}\,J/_{\circ K}$ (Boltzmann's constant)

T_0 is $290°K$ (source temperature proposed by Harold Friis)

B is network bandwidth (Hz)

G is network gain

As a result, Equation 5.5 defines N_i as proportional to B; however, both the numerator and the denominator have the term B. Since B is present in the numerator and

denominator it can be cancelled out, resulting in F being independent of B. Equation 5.5 is the standard definition of noise factor according to the Institute of Electrical and Electronics Engineers (IEEE) [15]. Simply, F defines the ratio of the total noise power output (P_{no}) to the noise power at the input (P_{ni}) when the source temperature is 290K, as shown in Equation 5.6.

$$F = \frac{P_{no}}{P_{ni}}|_{T=290K} \tag{5.6}$$

5.2.2 Noise Temperature (T_e)

The previous section defines how noise affects a network at the reference source temperature (T_0). However, it is unrealistic for noise effect to always be calculated at a certain temperature. The temperature variation must be considered as close as possible to the temperature in a real-life situation to evaluate the noise level. Therefore, the effective input noise temperature (T_e) describes the noise performance of a device. Assuming that T_e is the temperature of an ideal device that provides no noise except for N_a, the definition is shown as Equation 5.7 [15].

$$T_e = \frac{N_a}{KGB} \tag{5.7}$$

The Equation 5.7 can be rewritten in terms of F as shown in Equation 5.8.

$$T_e = T_0(F - 1) \tag{5.8}$$

Even though the NF is a universal way to interpret the noise effect, the source temperature is fixed at 290 K and is not completely accurate. Equation 5.8 is helpful for designers to evaluate the system's performance at the given temperature.

5.3 Network Gain (G)

Network gain (G) plays an essential role in noise factor as shown in Equation 5.5. The input power can be presented as KGT_0B, which represents the available and maximum power that can be delivered to the load. However, if the network has a considerable input mismatch, the actual power transferred to the network would be much less than expected. In this case, any power loss can be explained by the reflection coefficient ($\Gamma_{in}, \Gamma_s, \Gamma_{out}, \Gamma_L$) in a 2-port network [15], as shown in Figure 5-2.

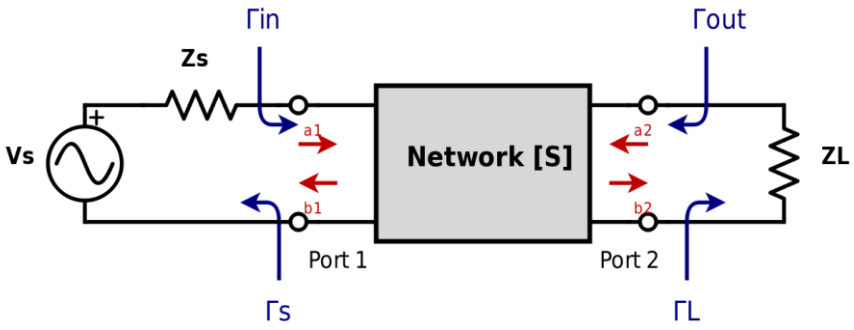


Figure 5-2 For a 2-port network, the input and output travelling waves are measured in a Z_0 system. The b_1 and b_2 equation are shown in Equation 4.13 and 4.14. Adapted from [15]

Consider a network with the source and load reflection coefficients Γ_s and Γ_L measured in a Z_0 system, as shown in Equation 5.9 and 5.10 (assuming $Z_0 = 50\ \Omega$ in RF circuits) as shown in Figure 5-3.

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{5.9}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{5.10}$$

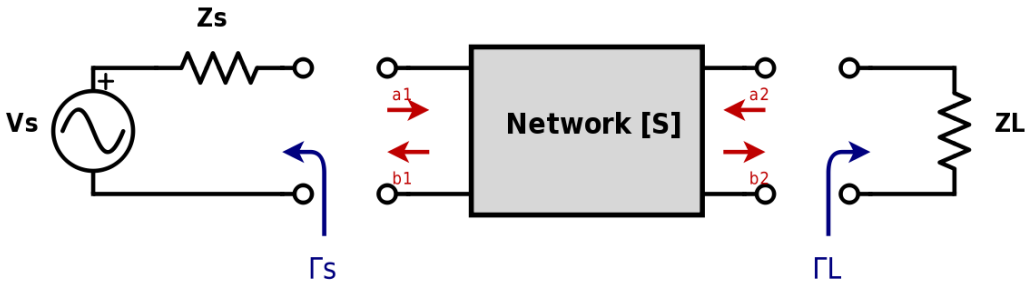


Figure 5-3 The reflection coefficients, Γ_s and Γ_L, are measured separately. Adapted from [15]

Finding the value of Γ_s and Γ_L is needed to define the Γ_{in} and Γ_{out} in terms of S-parameters, Γ_L and Γ_s using Equation 4.13 and 4.14. As a result, the Γ_{in} and Γ_{out} can be expressed as Equation 5.11 and 5.12.

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{5.11}$$

$$\Gamma_{out} = \frac{b_1}{a_2} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \tag{5.12}$$

The defined parameters and coefficients are used to define the power, transducer, available gains, and insertion gains that will be introduced in the following sections [15].

5.3.1 Power Gain (G_p)

As shown in Figure 5-4, power gain (G_p) is defined as the ratio of the power delivered to the load (P_L) to the power delivered to the network from the source (P_{in}), as shown in Equation 5.13 [15].

$$G_p = \frac{P_L}{P_{in}} \tag{5.13}$$

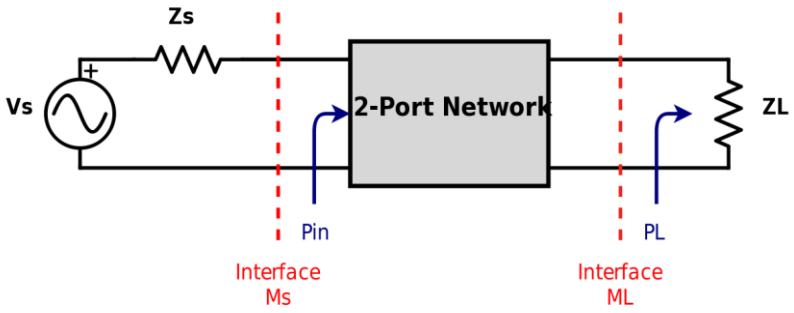


Figure 5-4 A 2-port network indicates that the G_p is obtained from the network input to the load. Adapted from [15]

The P_L and P_{in} in Equation 5.13 can be written in terms of Γ_L and Γ_{in} as shown in Equation 5.14 and 5.15 [15].

$$P_L = \frac{1}{2}|b_2|^2(1 - |\Gamma_L|^2) \tag{5.14}$$

$$P_{in} = \frac{1}{2}|a_1|^2(1 - |\Gamma_{in}|^2) \tag{5.15}$$

Where $b_2 = \frac{S_{21}a_1}{1-S_{22}\Gamma_L}$, therefore, Equation 5.13 can be expressed as Equation 5.16 [15].

$$G_p = \frac{1}{1 - |\Gamma_{in}|^2}|S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{5.16}$$

5.3.2 Transducer Gain (G_t)

As shown in Figure 5-5, transducer gain (G_t) is defined as the ratio of the power delivered to the load (P_L) to the maximum power available from the source (P_{as}). However, there is an interface (M_s) that is also known as the source mismatch factor between the source and network input. The M_s can be defined in Equation 5.17, which is interpolated to express G_t, as shown in Equation 5.18 [15].

$$M_s = \frac{P_{in}}{P_{as}} = \frac{(1-|\Gamma_s|^2)(1-|\Gamma_{in}|^2)}{|1-\Gamma_s\Gamma_{in}|^2} \tag{5.17}$$

$$G_t = \frac{P_L}{P_{as}} = \frac{P_L}{P_{in}}\frac{P_{in}}{P_{as}} = G_p M_s \tag{5.18}$$

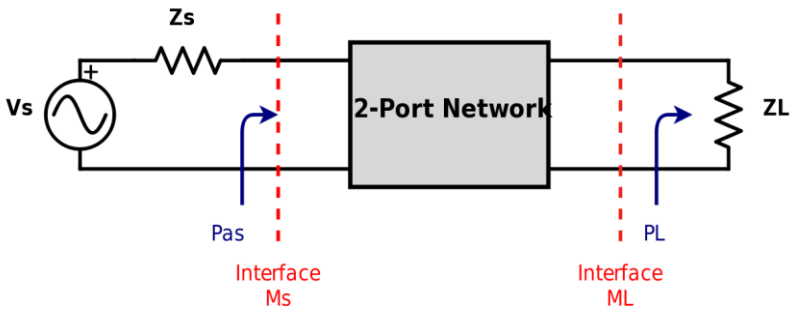


Figure 5-5 A 2-port network indicates that the G_t is obtained from the source to the load. Adapted from [15]

Finally, combine Equation 5.17 and 5.18 to obtain Equation 5.19 [15].

$$G_t = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \tag{5.19}$$

5.3.3 Available Gain (G_a)

As shown in Figure 5-6, available gain (G_a) can be defined as the ratio of the output network's available power (P_{ao}) and the source's available power (P_{as}). The interface between network output and load, also known as load mismatch factor (M_L), is defined as Equation 5.20. The M_L must be considered in G_a as shown in Equation 5.21 [15].

$$M_L = \frac{P_L}{P_{ao}} = \frac{(1-|\Gamma_L|^2)(1-|\Gamma_{out}|^2)}{|1-\Gamma_{out}\Gamma_L|^2} \tag{5.20}$$

$$G_a = \frac{P_{ao}}{P_{as}} = \frac{P_L}{P_{as}}\frac{P_{ao}}{P_L} = \frac{G_t}{M_L} \tag{5.21}$$

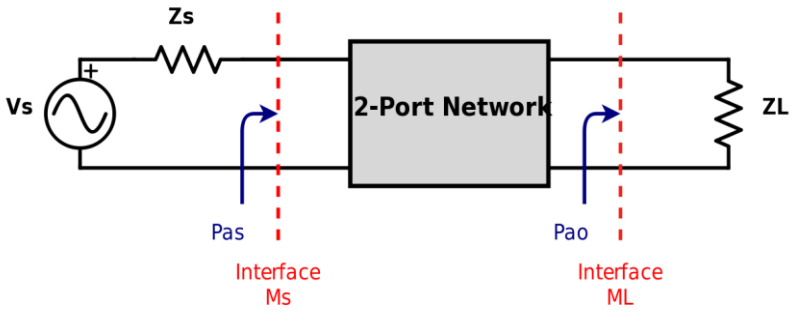


Figure 5-6 A 2-port network indicates that the G_a is obtained from the source to the network output. Adapted from [15]

Finally, combine Equation 5.20 and 5.21 to obtain Equation 5.22 [15].

$$G_a = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \tag{5.22}$$

5.4 Linearity

In addition to noise, gain, and matching network, linearity is an important factor in LNA design. LNA not only amplifies the signal but also remains as a linear operation. Furthermore, the LNA must uphold linearity for both weak and strong signals in the presence of an interfering signal. There are two main design properties of linearity which are 1-dB compression point (P_{1dB}) and third-order intercept Point ($IP3$) [16]. These properties will be introduced to improve the LNA design.

5.4.1 1-dB Compression Point (P_{1dB})

An amplifier has a solid gain at a specific frequency range in which the input and output power relationship would be linear, as shown in Figure 5-7. The slope represents the power gain in dBm. As the input power gradually increases, the output power saturates. At P_{1dB}, the amplifier enters the compression region in which output power

increases can no longer occur for input power increase. It means that while the strong signal is received, the amplifier becomes non-linear and produces signal distortion, harmonics, and potentially intermodulation products [16].

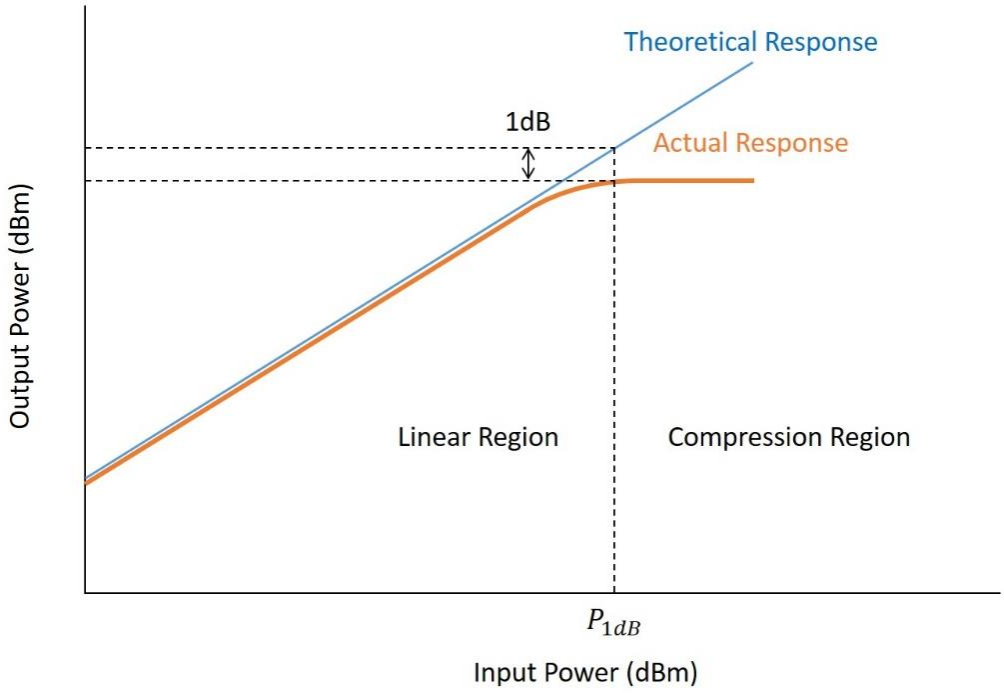


Figure 5-7 The P_{1dB} point is the input power that causes the power gain to decrease 1 dB from the theoretical response. Adapted from [16]

A sinusoid input signal is applied to a non-linear system to explain the P_{1dB}, as shown in Equation 5.23. The output signal can be presented as Equation 5.24, including $\cos \omega t$, $\cos 2\omega t$, and $\cos 3\omega t$ as Equation 5.25 [16].

$$x(t) = A \cos \omega t \tag{5.23}$$

$$y(t) = \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t \tag{5.24}$$

$$y(t) = \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4}) \cos \omega t + \frac{\alpha_2 A^2}{2} \cos 2\omega t + \frac{\alpha_3 A^3}{4} \cos 3\omega t \tag{5.25}$$

In Equation 5.25, the desired signal is $\cos \omega t$, others are the byproduct of the input signal that is also called harmonic distortion [16]. Notice that the sign of $\alpha_1 \alpha_3$ can change the characteristics of the amplifier. If the $\alpha_1 \alpha_3 > 0$, the entire circuit would be expansive which means that the output signal will keep increasing with the input signal. However, this characteristic is not likely to appear in the metal-oxide-semiconductor field-effect-transistor (MOSFET), unless it is a bipolar junction transistor (BJT), since MOSFET saturates at a certain point. Therefore, assuming that $\alpha_1 \alpha_3 < 0$, the circuit has the compressive characteristics that are more suitable for LNA design.

Finally, the definition of P_{1dB} is 1dB below expected output power by giving input signal as shown in Equation 5.26 [16].

$$10 \log \left| \alpha_1 + \frac{3\alpha_3 A^2}{4} \right| = 10 \log |\alpha_1| - 1dB \tag{5.26}$$

where:

$\alpha_1 + \frac{3\alpha_3 A^2}{4}$ is actual power response

α_1 is expected power response

5.4.2 Third-Order Intercept Point ($IP3$)

Assuming that the input of an amplifier is a sinusoid signal, when the amplifier becomes non-linear, the output signal will be harmonics such as $\cos 2\omega t$ and $\cos 3\omega t$, as shown in Equation 5.25 [16]. The higher harmonics are not a significant interference since they are usually not in the bandwidth. However, non-linearity will also produce a mixing effect of two or more signals.

If received signals are within the adjacent frequency range, intermodulation products are produced which can occur within the particular bandwidth, as shown in Figure 5-8 [16]. Specific sum and difference frequencies from the received signal in the adjacent frequency range are known as intermodulation products. These intermodulation products cannot be filtered out since they will eventually convert to interfering signals along with the desired signals. Several approaches such as control of biasing, signal levels, and other factors ensure the highest possible linearity and significantly reduce the intermodulation distortion (IMD) products [16].

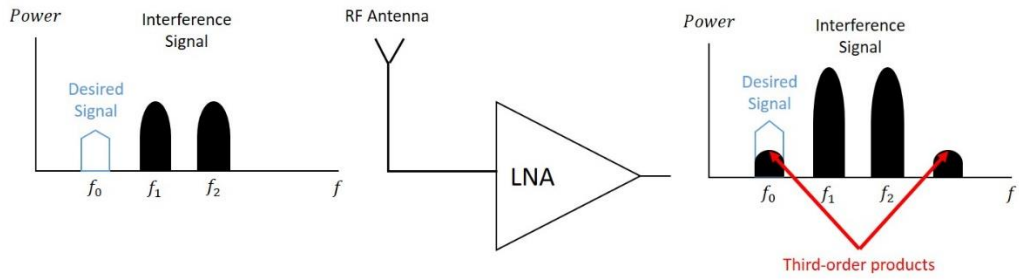


Figure 5-8 Corruption due to third-order intermodulation. Adapted from [16]

Figure 5-9 shows two input signals f_1 and f_2 occuring within the amplifier bandwidth. When distortion occurs, new signals $f_2 - f_1$ and $f_2 + f_1$ are created. In most cases, these can be filtered out. However, these signals will also combine with the second, third, and even higher harmonics to yield a wide range of possibly interfering signals with the amplifier bandwidth. Most of the complications occur in the third-order products which are in the frequency range of $2f_1 - f_2$ and $2f_2 - f_1$.

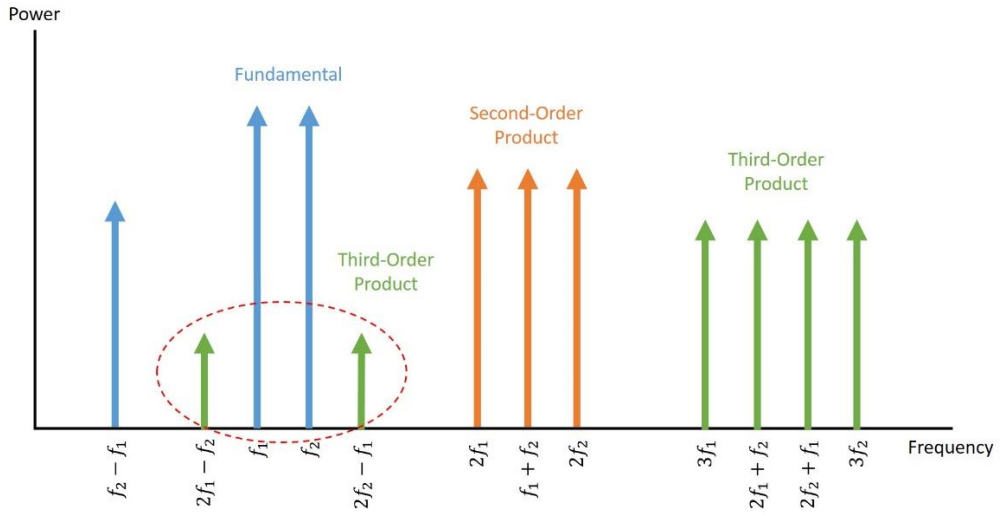


Figure 5-9 Two input signals, f_1 and f_2, amplified by an amplifier that produces the second and third harmonics. Adapted from [16]

Finally, IP3 is defined using the Equation 5.25. In Figure 5-10, the linear portions of the two gain curves extend so that the first-order (or fundamental) and the third-order signal will meet at the IP3. The IP3 is where the first-order input is equal to the third-order input as shown in Equation 5.27. The corresponding input and output are called the third-order input intercept point (IIP3) and third-order output intercept point (OIP3) [16].

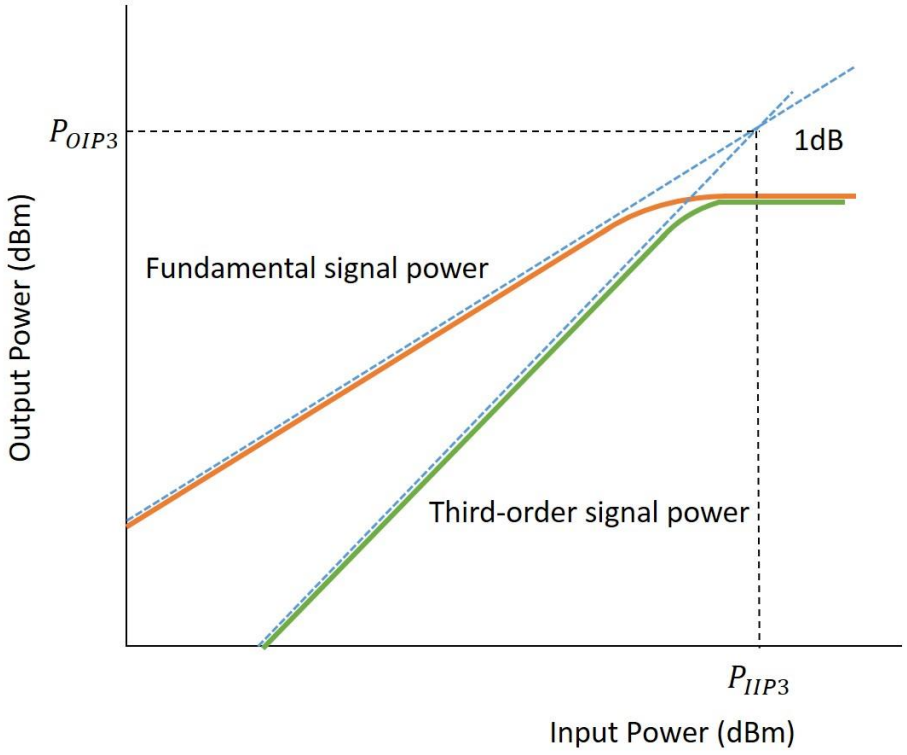


Figure 5-10 The IP3 is a theoretical point at which the third-order distortion signal amplitudes equal the input signals. Adapted from [16]

$$| \alpha_1 P_{IIP3}| = \left| \frac{3\alpha_3 {P_{IIP3}}^3}{4} \right| \tag{5.27}$$

We can relocate the P_{IIP3} to the left hand side as shown in Equation 5.28.

$$P_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{5.28}$$

Notice that IP3 is a theoretical point that is never achieved in real-world conditions. However, it is helpful for designers when determining the linearity condition of an amplifier.

5.5 Summary

In Chapter 5, three design specifications of LNA are introduced. A successful LNA must be equipped with high gain, low NF, and high linearity. In section 5.3, different definitions of gain have been discussed; the critical key to achieve high gain is to have maximum power transfer. A well-designed input and output matching network are necessary to achieve the highest possible gain.

Chapter 6

Schematic Design

6.1 Introduction

In Chapter 6, with all the necessary elements, the physical schematic design will be presented and simulated in the Cadence ADE with GPDK 45 nm process technology. The entire LNA circuit will be broken down into five parts: topologies, source degeneration feedback, input matching network, output matching network, and biasing circuits. Furthermore, the key performance factors, such as NF, gain, P1dB, and IIP3 will be shown in Chapter 6 to ensure that the design satisfies the criteria of the BLE front-end receiver. The specifications of LNA design is listed in Table 1.

Table 1 LNA Design Specifications

Parameters	**Specifications**
Power Supply	1-3 V
Power Dissipation	4-20mW
Input and Output Impedance	50 Ω
Gain	> 13.4 dB
NF	< 3 dB
IIP3	> -10 dBm

Based on references [17][18][19][20][21][22]

6.2 Topologies Consideration

There are three prevailing LNA topologies, which are common source (CS), common gate (CG), and cascode. The characteristics of the three topologies are shown in Table 2 [23]. The cascode amplifier is the most popular solution for LNA since it provides the highest gain over the widest bandwidth with only a slight sacrifice in NF performance and design complexity. The structure of a cascode amplifier combines a CS stage and a

CG stage. The CS stage provides the greatest stability which has better sensitivity to process, temperature variation immunity, power supply, and component variations [23]. Therefore, a cascode amplifier is implemented in the LNA design of the BLE front-end receiver.

Table 2 Characteristics of CS, CG, and Cascode Topologies

Characteristic	**CS**	**CG**	**Cascode**
NF	Lowest	Rises rapidly with frequency	Slightly higher than CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly Broad	Broad
Stability	Often requires compensation	Higher	Higher
Reverse Isolation (S12)	Low	High	High
Stability	Greater	Lesser	Lesser

Based on references [23]

There are four function blocks in a cascode LNA. These blocks are source degeneration feedback, input matching network, biasing circuit, and output matching network. The schematic can be shown in Figure 6-1. Each block has different contributions that will be introduced in the following sections.

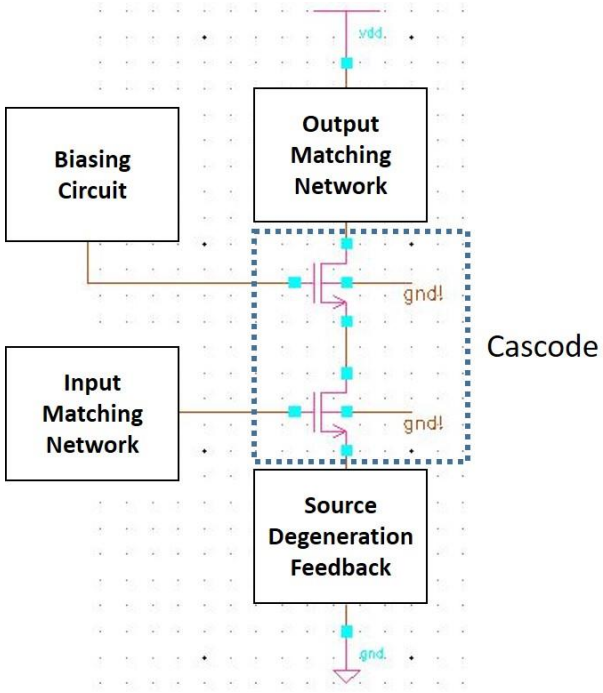
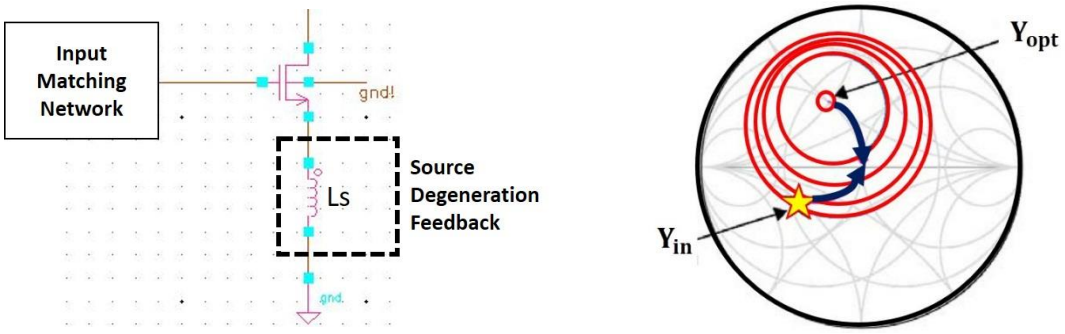


Figure 6-1 Structure of a cascode LNA with four different function blocks

6.3 Source Degeneration Feedback

The source degeneration feedback can be implemented by placing a source inductor (L_s) as shown in Figure 6-2 (a). The purpose of the feedback circuit is to acquire the optimized admitance (Y_{opt}) and concurrently converges on input admitance (Y_{in}) which can be shown in the Smith chart in Figure 6-2 (b)[23]. Y_{opt} is the input admitance of the LNA at which the minimum noise factor (F_{min}) occurs. The value of L_s must be carefully designed to avoid instability within the system, which is caused by too much or too little feedback.



(a) (b)

Figure 6-2 (a) Inserting a source inductor as source degeneration feedback. (b) The Smith chart indicates that the source generation feedback can help optimize admittance Y_{opt} simutaneously converge on Y_{in}.

The Smith chart can be used to find the minimum noise figure (NF_{min}) and maximum gain; however, in a non-ideal case, the maximum gain and NF_{min} will not occur at the same impedance state. It is the trade-off between gain and NF in which the designer must find the balance to satisfy both gain and NF based on the given specification table. Overall, the source degeneration feedback improves LNA's linearity and stability in exchange for some amount of gain.

6.4 Input Matching Network

The main purpose of input matching network is to achieve the maximum power transfer rate. As mentioned in Chapter 3, the maximum power transfer happens when impedance matches. The input small-signal model of the LNA is shown in Figure 6-3. The LNA is connected to a voltage source that simulates the received signals from the antenna. The source impedance (Z_s), the antenna's resistance, can be specified as 50 Ω. Therefore, the LNA's input impedance (Z_{in}), must match the exact 50 Ω in order to transfer the maximum power to the next stage of the system.

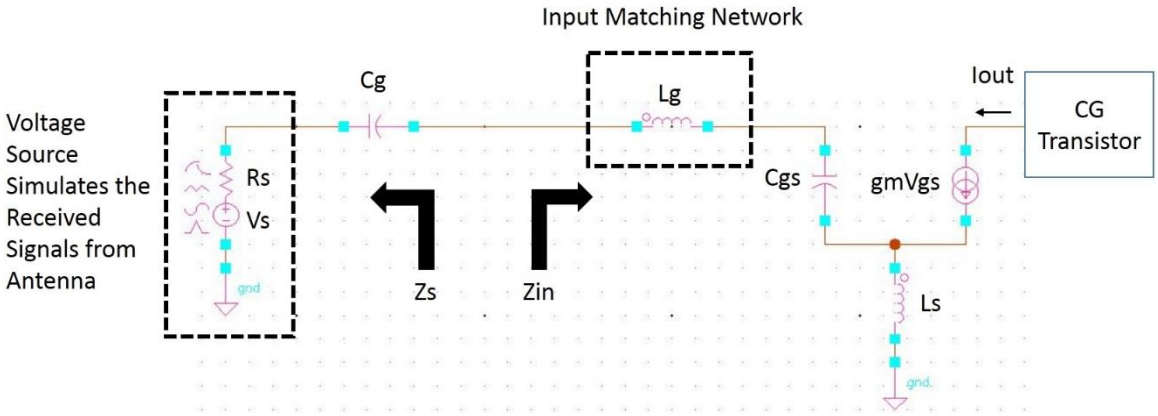


Figure 6-3 The small-signal model for the LNA

In Figure 6-3, gate inductor (L_g) is marked as the input matching network. The designer can choose from a single component to multiple components, such as L-match, T-match, and π-match for different applications. Z_{in} can be expressed as Equation 6.1 [24].

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega}\frac{1}{C_{gs}} + \frac{gmL_s}{C_{gs}} \tag{6.1}$$

where:

C_{gs} is the capacitor between gate and source in CS amplifier

L_s is the source inductor

g_m is the transconductance of CS amplifier

Since the Z_{in} is equal to 50 Ω, the imaginary part of the impedance is zero. As a result, L_g and L_s can be obtained by Equation 6.2 and 6.3 [24].

$$L_g = \frac{1}{\omega^2(C_{gs} + C_{ex})} - L_s \tag{6.2}$$

$$L_s = Z_{in}\frac{(C_{gs} + C_{ex})}{gm} \tag{6.3}$$

In Equation 6.2, ω is the operation frequency in which the LNA can reach the best performance. For the BLE front-end receiver, the center frequency (f_c) is set as 2.44 GHz. The C_{gs} and g_m can be found by ADE DC analysis. The DC operating points of the M1 transistor show that the C_{gs} is 20.1198 fF and g_m is 12.2042 ms.

Note that an external capacitor (C_{ex}) can be added in parallel to C_{gs} to help improve the linearity and NF in exchange for the gain performance. The drawback of the C_{ex} can be shown in Figure 6-4, Figure 6-5, and Figure 6-6.

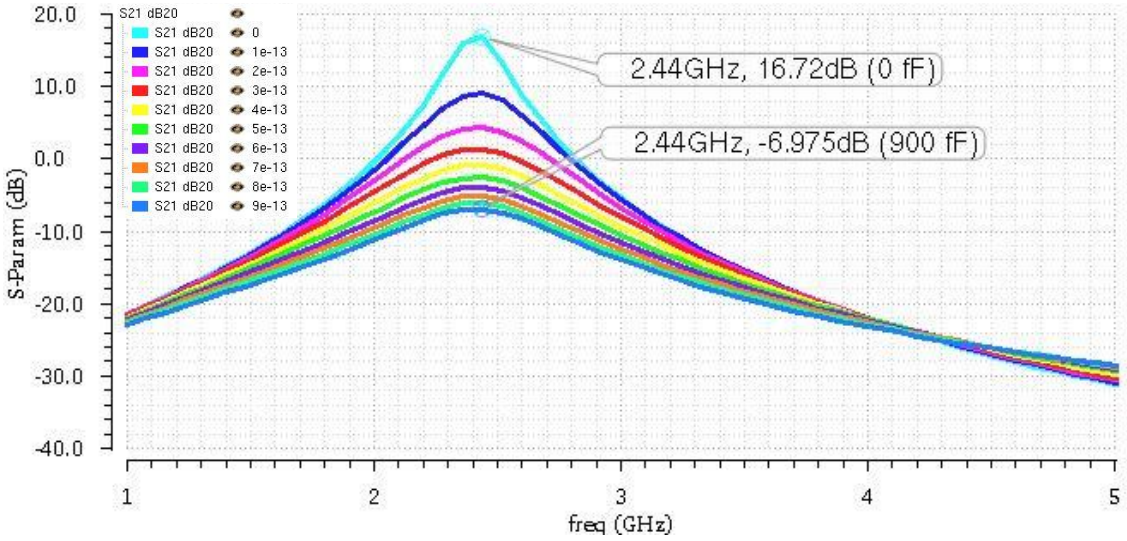


Figure 6-4 S-parameter, S21, with C_{ex} varying from 0 fF to 900 fF

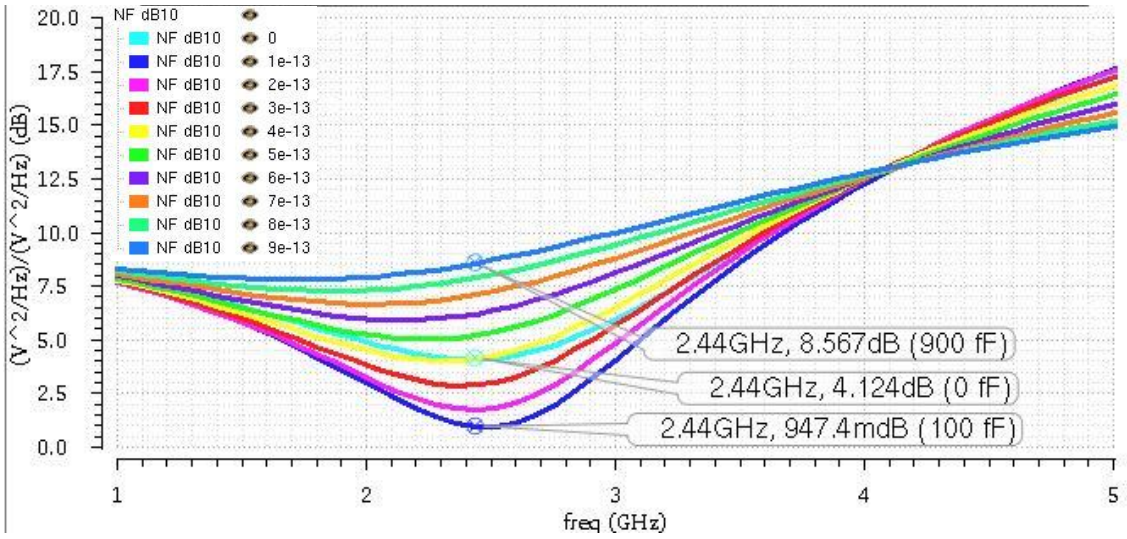


Figure 6-5 NF with C_{ex} varying from 0 fF to 900 fF

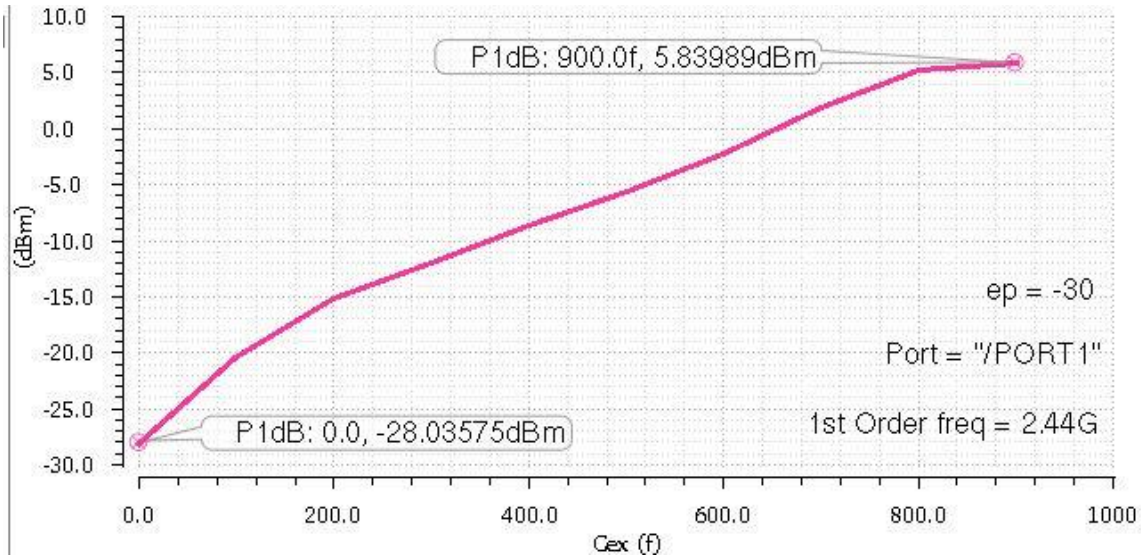


Figure 6-6 P1dB with C_{ex} varying from 0 fF to 900 fF

Without an additional C_{ex}, the maximum gain is 16.72 dB, NF is 4.124 dB, and P1dB is -28 dBm. Input matching is a compromise between linearity and gain; however, the additional C_{ex} is needed to satisfy the BLE specifications.

6.5 Output Matching Network

To design the output circuit, one must know the input impedance of the next stage ($Z_{in,2}$) and use the maximum power transfer theory to design the output impedance (Z_{out}) in the presented circuit, as shown in Figure 6-7. Assuming that the $Z_{in,2}$ is equal to 50 Ω, not only the real part of the Z_{out} has to be 50 Ω, but also the imaginary part has to be zero to operate at the resonant frequency. Therefore, the output matching network must be equipped with resistor (R_d), inductor (L_d), and capacitor (C_d).

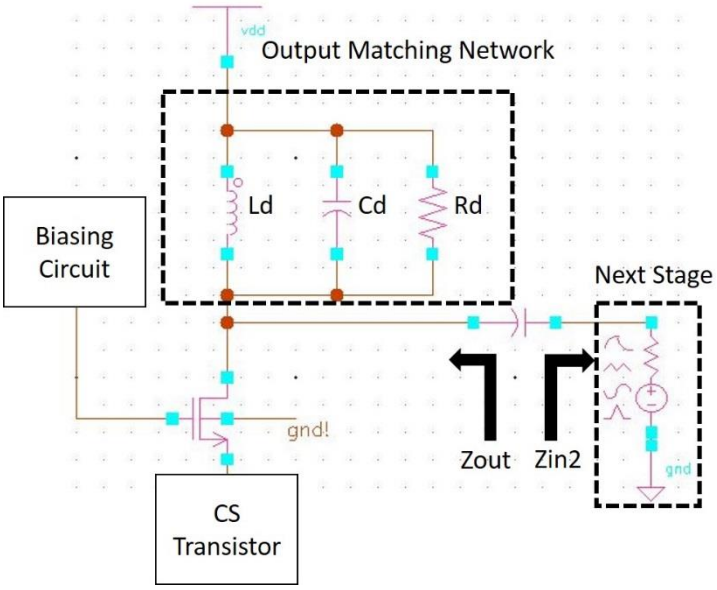


Figure 6-7 The output matching network of the LNA

At $f_c = 2.44$ GHz, Z_{out} and $Z_{in,2}$ are expressed as Equation 6.4. The C_d and L_d will cancel each other out.

$$Z_{out} = Z_{in,2} = R_d = 50\ \Omega \tag{6.4}$$

The C_d ranges from 100fF to 1pF while the L_d is changed according to Equation 6.5. In Figure 6-8, the effect of the load capacitor, in terms of gain, NF, and linearity do not change significantly.

$$L_d = \frac{1}{\omega^2 C_d} \tag{6.5}$$

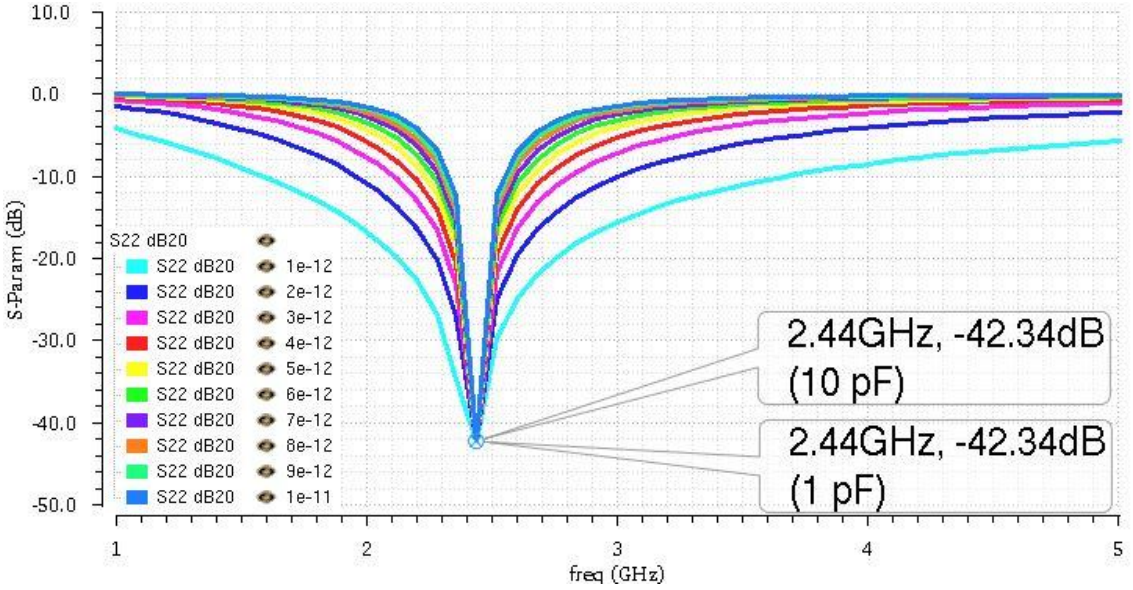


Figure 6-8 The S-parameter, S22, with C_d varying from 1 pF to 10 pF

In Figure 6-8, the S22 shows that the output reflection coefficient falls on -42.34 dB, even the C_d varies. However, the effective channel of Bluetooth ranges from 2.402 to 2.480 GHz. The C_d is chosen as 1 pF to have the same selectivity as Bluetooth.

6.6 Biasing Circuit

In BLE design, low energy is essential for the system to have longer operation periods without charging. The biasing circuit must constrain the power consumption to be close to 1 mW. In this design, the supply voltage (Vdd) is set as 1V, since there are two

transistors (CS and CG) that need to be biased. The current mirror is implemented to constrain the current flow to fix the total current close to 1 mA, as shown in Figure 6-9.

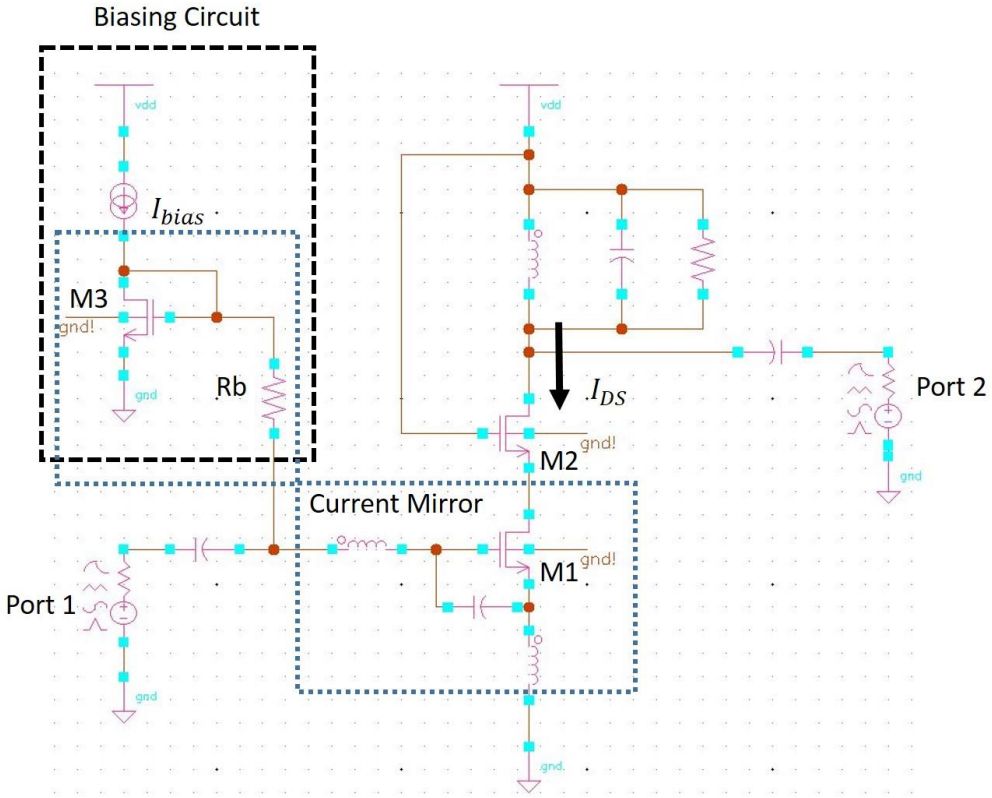


Figure 6-9 The biasing circuit for the LNA design

The M3 and M1 transistors form a current mirror. The I_{bias} is the reference current for I_{DS} which is the current flow through cascode transistors M1 and M2. The ratio of the current flow depending on the transistor's width of M2 and M1. In order to constrain the power to 1 mW, the I_{bias} must be properly designed so that M1, M2, and M3 can both operate in saturation mode. The current equation for I_{bias} when M3 operates in saturation mode is shown in Equation 6.6 [25].

$$I_{bias} = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L}(V_{gs3} - V_{th3})^2 \tag{6.6}$$

In Equation 6.6, the V_{gs3} must be greater than not only V_{th3} but also V_{th1} to drive the M3 and M1 both in saturation mode. In order to find the best biasing point, the W_3 was swept from 1 um to 10 um. The I_{bias} was applied from 20 uA to 200 uA to observe the V_{gs3} which is greater than V_{th3} and V_{th1}, as shown in Figure 6-10. The corresponding value is shown in Table 3.

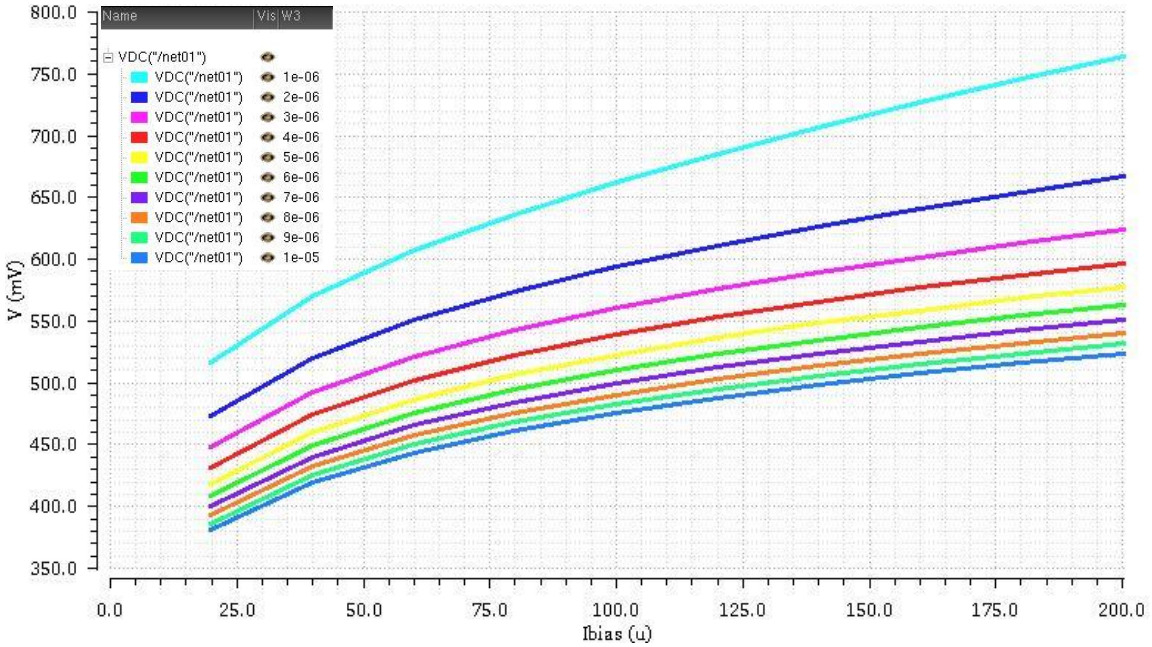


Figure 6-10 The V_{gs3} with I_{bias} varying from 20 uA to 200 uA and W_3 varying from 1 um to 10 um

Table 3 The Corresponding Values for V_{gs3} with Varied I_{bias} and W_3

Ibias (uA)	**Vgs3 (V), W_3 (um)**									
	W_3=1	W_3=2	W_3=3	W_3=4	W_3=5	W_3=6	W_3=7	W_3=8	W_3=9	W_3=10
20	0.52	0.47	0.45	0.43	0.42	0.41	0.4	0.39	0.39	0.38
40	0.57	0.52	0.49	0.47	0.46	0.45	0.44	0.43	0.43	0.42
60	0.61	0.55	0.52	0.5	0.49	0.48	0.47	0.46	0.45	0.44
80	0.64	0.57	0.54	0.52	0.51	0.49	0.48	0.48	0.47	0.46
100	0.66	0.59	0.56	0.54	0.52	0.51	0.5	0.49	0.48	0.48
120	0.68	0.61	0.58	0.55	0.54	0.52	0.51	0.5	0.5	0.49
140	0.71	0.63	0.59	0.57	0.55	0.53	0.52	0.51	0.51	0.5
160	0.73	0.64	0.6	0.58	0.56	0.54	0.53	0.52	0.52	0.51
180	0.75	0.65	0.61	0.59	0.57	0.55	0.54	0.53	0.52	0.52
200	0.76	0.67	0.62	0.6	0.58	0.56	0.55	0.54	0.53	0.52

DC analysis in Cadence ADE is used to find V_{th3}, which varies from 0.51 V to 0.519 V. Additionally, the same method can be applied to find V_{th1} which varies from 0.498 V to 0.501 V. Therefore, the V_{gs3} must be greater than 0.52 V in Table 3, the shaded areas of the table represent the values that do not satisfy the conditions.

The next step would be the power consumption of the circuit which is set as 1 mW. As shown in Table 4, the power consumption is greater than 1.1 mW and is presented in the shaded parts of the table. The shaded area shown in the table will not be considered as operation points.

Table 4 The Corresponding Values for Power Consumption of the Circuit with Varied I_{bias} and W_3

Ibias (uA)	**P (mW), W_3 (um)**									
	W_3=1	W_3=2	W_3=3	W_3=4	W_3=5	W_3=6	W_3=7	W_3=8	W_3=9	W_3=10
20	1.01	0.61	0.45	0.36	0.31	0.27	0.24	0.22	0.20	0.19
40	1.77	1.07	0.79	0.64	0.54	0.47	0.42	0.39	0.35	0.33
60	2.46	1.49	1.10	0.89	0.76	0.66	0.59	0.54	0.50	0.46
80	3.11	1.88	1.39	1.13	0.96	0.84	0.75	0.69	0.63	0.59
100	3.72	2.25	1.67	1.36	1.16	1.01	0.91	0.83	0.76	0.71
120	4.31	2.61	1.94	1.58	1.35	1.18	1.06	0.96	0.89	0.83
140	4.87	2.96	2.21	1.79	1.53	1.34	1.20	1.10	1.01	0.94
160	5.41	3.30	2.46	2.00	1.71	1.50	1.35	1.23	1.13	1.05
180	5.93	3.63	2.71	2.21	1.88	1.66	1.49	1.36	1.25	1.16
200	6.42	3.95	2.95	2.41	2.05	1.81	1.62	1.48	1.37	1.27

Finally, according to Table 3 and Table 4, one must choose a biasing point among all the eligible points, which are labeled in yellow. The point ($I_{bias} = 20\ uA, W_3 = 1um$) is chosen since it is closest to the 1 mW power dissipation. In this case, the width of M1 and M2 were estimated using Equation 6.7. The W_1 and W_2 are given the value of 37.5 um.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L}(V_{gs1} - V_{th1})^2 \tag{6.7}$$

6.7 Simulation Results

The final schematic is presented, in which the input matching network, source degeneration feedback, output matching network, and the biasing network are put together to complete the entire LNA design, as shown in Figure 6-11. The LNA's performance is provided in Table 5. Four factors determine the performance, which are power consumption, gain, NF, and linearity.

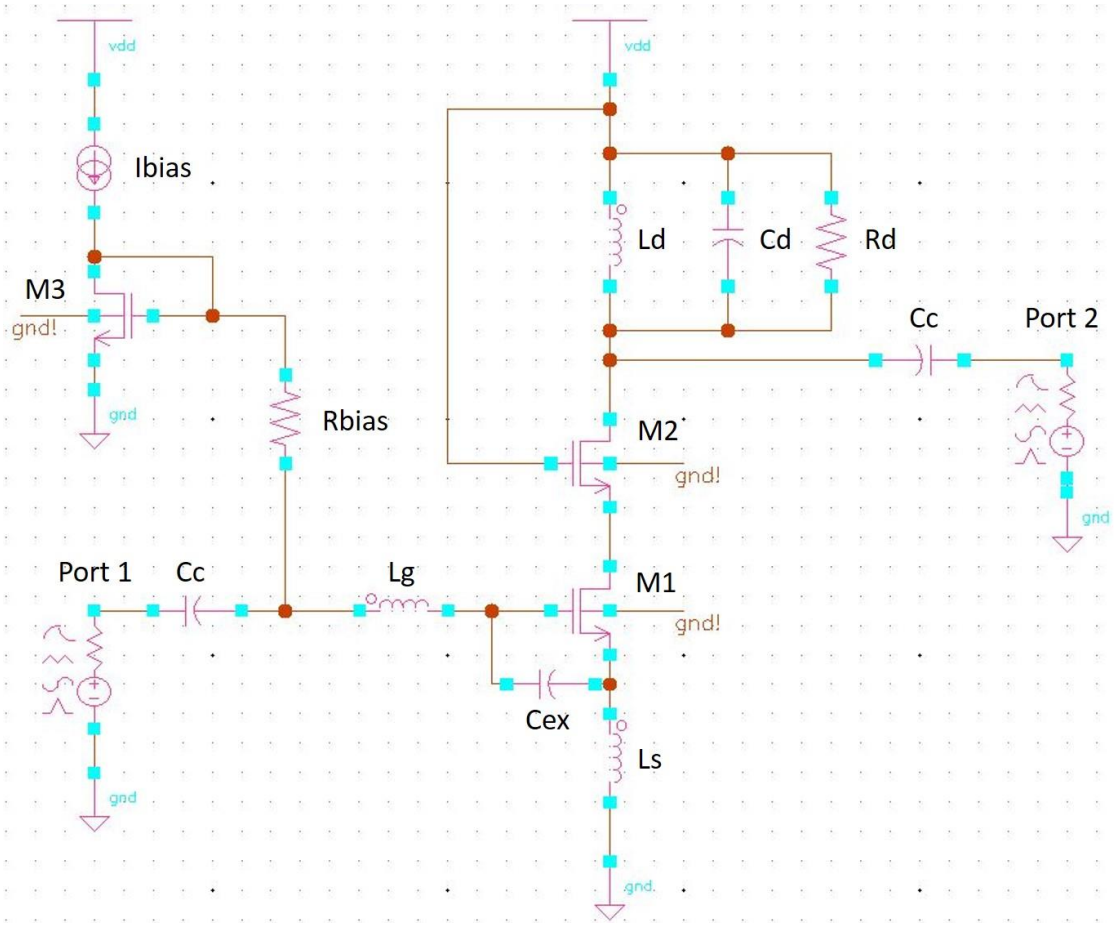


Figure 6-11 The schematic of the LNA design

Table 5 LNA Design Performance

Parameters	Specifications
Power Supply (V)	1
Power Dissipation (mW)	1.01
Gain (dB)	14.53
NF/NF min	0.98/0.56
P1dB (dBm)	-17.32
IIP3 (dBm)	-10.67

The Gain, NF, P1dB, and IIP3 are shown in Figure 6-12, Figure 6-13, Figure 6-14, and Figure 6-15.

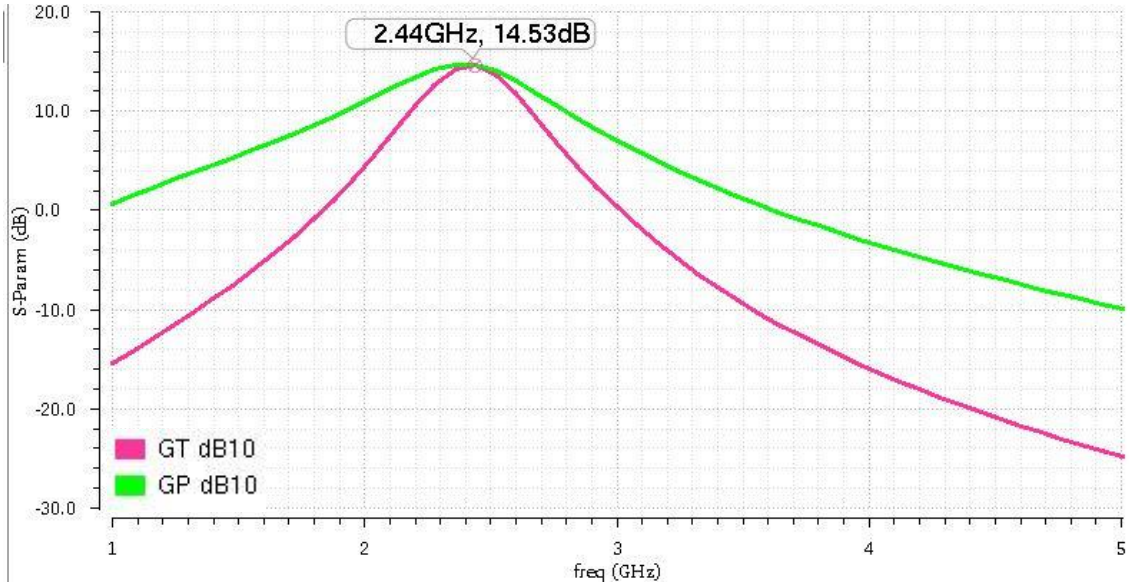


Figure 6-12 The maximum gain of the LNA at 2.44 GHz is 14.53 dB

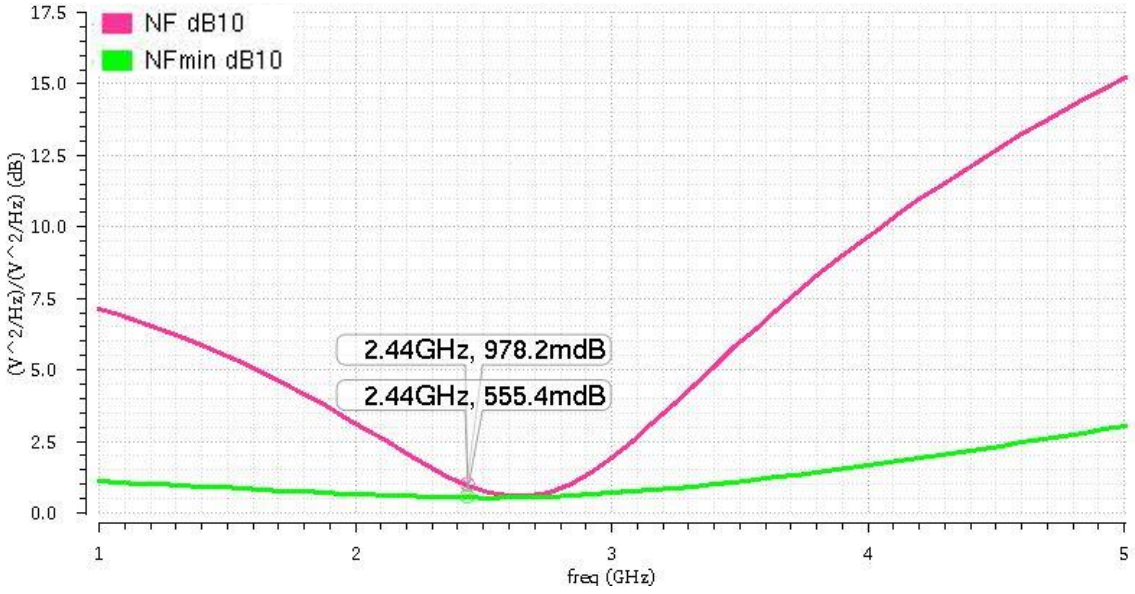


Figure 6-13 The NF and NF minimum of the LNA

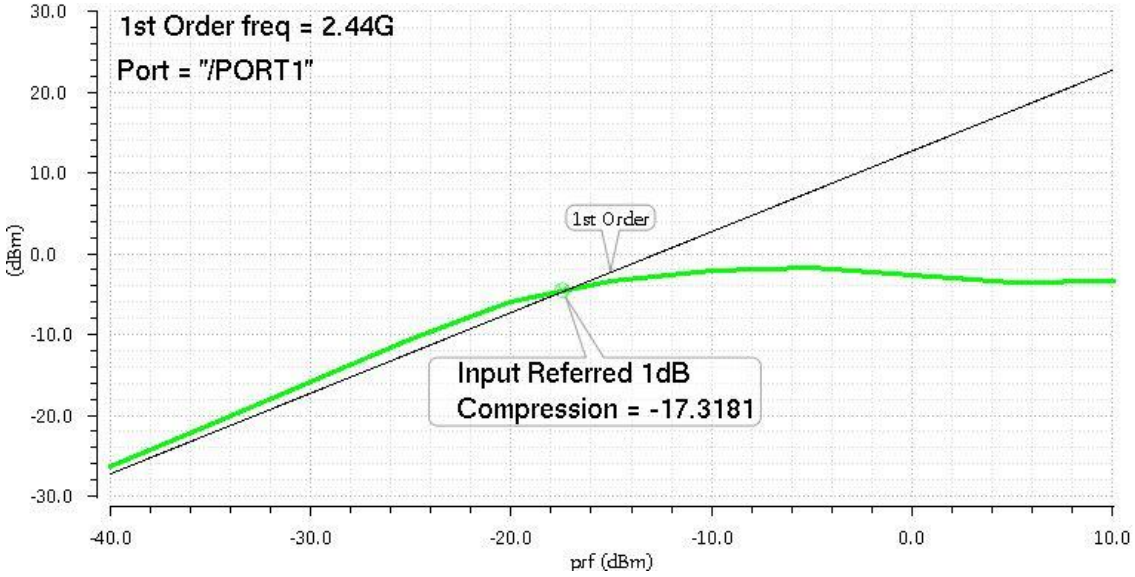


Figure 6-14 The P1dB of the LNA is -17.3181 dB

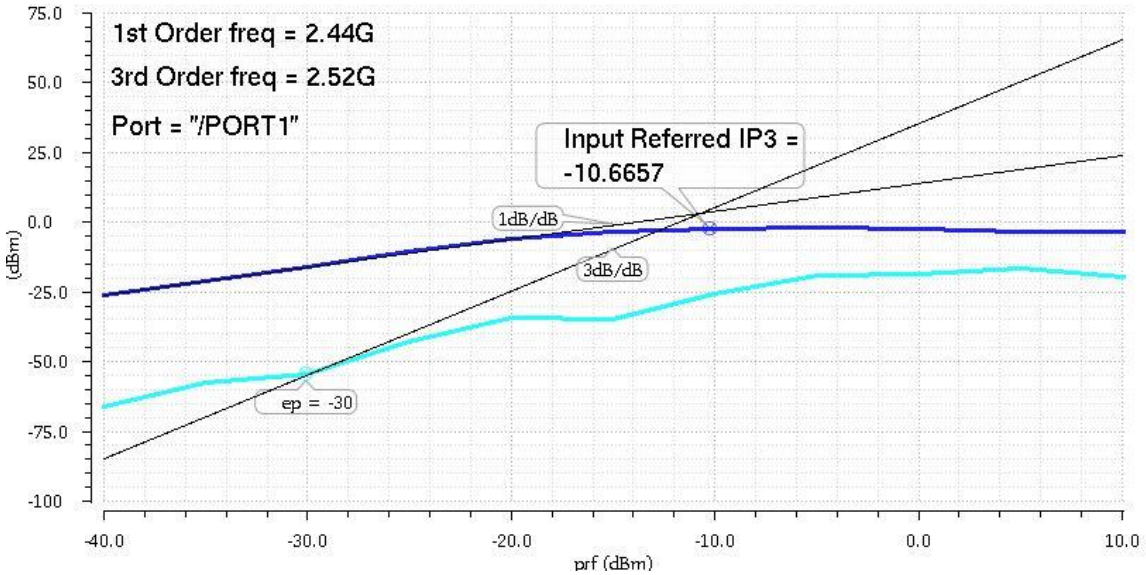


Figure 6-15 The IIP3 of the LNA is -10.6657 dB

6.8 Performance Summary

The comparison of LNA performance is shown in Table 6.

Table 6 LNA Comparison to Other Works

[Ref]	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Frequency (GHz)	Technology
[17]	22	2.5	-10	12	2.5	0.35 um
[18]	19.8	3	4.5	22.4	2.4	0.35 um
[19]	15	2.2	1.3	7.2	2.4	0.25 um
[20]	13.4	3	0	4.5	2.5	0.25 um
[21]	20.343	1.98	5	7.33	2.4-2.5	0.13 um
[22]	22.1	1.47	-8.1	11.1	2.4	0.18 um
This Work	**14.53**	**0.98**	**-10.67**	**1.01**	**2.44**	**45 nm**

Even though the IIP3 value was relatively lower than other works, the NF was the lowest. By using the 45 nm technology, the smallest technology was implemented. Moreover, the power consumption was extremely low among all the applications.

Chapter 7

Conclusion

7.1 Contribution

A low power LNA design was presented in this thesis for comparison to previous work [17][18][19][20][21][22]. The design reduced the power consumption to 1.01 mW which conserved more power for wireless applications. Additionally, the well-designed matching network for input and output allowed for the LNA to have the lowest NF which was 0.98 dB, and reasonable gain which was 14.53 dB. Although the gain was not the highest among previous work [17][18][19][20][21][22], the main goal of reducing power dissipation was achieved. Additionally, the 45 nm process technology was the smallest scale used in an LNA design which can save much space in an integrated circuit.

7.2 Future Work

Low-power LNA is the first step of the front-end design. To effectively complete the BLE front-end receiver, the emphasis of future work should focus on the design of a balun and a mixer, which are the second and third stages of the circuit. A balun is a circuit that transforms from a balanced transmission line to an unbalanced transmission line. The balun's purpose is that it can be utilized as a phase shifter, balance modulator, and balance mixer in antenna driving applications [26]. A mixer can provide high conversion gain and linearity in BLE front-end circuits [27]. With these two designs, we can improve the current front-end design in terms of gain and linearity.

7.3 Summary

This thesis includes an introduction to the key factors of BLE, an overview of the RF circuit theory, and the LNA design parameters. Each section provides detailed information and background knowledge to design a BLE front-end circuit. The thesis aimed for a design with low power dissipation that can be applied to BLE devices. The LNA circuit gave exceptionally low energy consumption and NF. Depending on different purposes of the application, the focus of the design can be chosen among power, gain, NF, and linearity.

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